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Photonic analog-to-digital coonversion using a robust symmetrical number system

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THESIS

PHOTONIC ANALOG-TO-DIGITAL CONVERSION USING A ROBUST SYMMETRICAL NUMBER SYSTEM

by

Adam S. Fisher

June 2005

Thesis Advisor:	Phillip E. Pace
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This design uses the RSNS preprocessing to encode the signal with the fewest number of comparators for any selected bit resolution. In addition to the efficiency of its use of comparators, the RSNS encoding has inherent Gray-code properties making it particularly attractive for eliminating any possible encoding errors. The RSNS encoding is combined with an optical infrastructure that offers high bandwidth and low insertion loss characteristics.

A full implementation was constructed and tested. The lack of a high-speed data acquisition device limited the results to examining the preprocessing and digital processing separately. With the system integration of a data acquisition device, a wideband direct digital antenna architecture can be demonstrated.

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PHOTONIC ANALOG-TO-DIGITAL CONVERSION USING A ROBUST SYMMETRICAL NUMBER SYSTEM

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EXECUTIVE SUMMARY

Analog-to-digital conversion has been widely researched in recent years. This stems from the increased capabilities that would be realized if an analog-to-digital converter (ADC) with a higher resolution and faster sampling rate was developed. Higher sampling rates, in particular, would allow for increased ultra-wideband and microwave signal collection applications. Optical processing techniques are recognized as one of the ways to accomplish the multi-Gb/s sampling rates necessary for such applications. Many unique architectures have been investigated to take advantage of the higher sampling rates that are available [1-10].

An implementation for a photonic analog-to-digital converter (ADC) based on a robust symmetrical number system (RSNS) was constructed and tested in this thesis. The analog signal to be converted is used to amplitude modulate light from a continuous-wave laser using three Mach-Zehnder interferometers (MZI). The Mach-Zehnder interferometers fold the input analog signal for a three-channel RSNS encoding. The folding waveforms are then detected and amplitude-analyzed by three separate comparator banks, the outputs of which are used to determine a digital representation of the analog signal.

This design uses the RSNS preprocessing to encode the signal with the fewest number of comparators for any selected bit resolution. In addition to the efficiency of its use of comparators, the RSNS encoding has inherent Gray-code properties making it particularly attractive for eliminating any possible encoding errors. The RSNS encoding is combined with an optical infrastructure that offers high bandwidth and low insertion loss characteristics.

A full implementation was constructed. The design consisted of two separate stages. The first stage consisted of the modulation and the optical infrastructure needed to produce three folding waveforms. The waveforms produced fell within the requirements of the RSNS encoding. A second stage was made up of a sampling circuit with three banks of comparators. This stage was tested using a variable DC voltage as the comparator inputs. In this way, the operation of the sampling circuit was verified. The lack of a

high-speed data acquisition device prevented the combination of the two stages. With the system integration of a faster data acquisition device though, a wideband direct digital antenna architecture can be demonstrated.

I. INTRODUCTION

A. BACKGROUND

Analog-to-digital conversion has been widely researched in recent years. This stems from the increased capabilities that would be realized if an analog-to-digital converter (ADC) with a higher resolution and faster sampling rate was developed. Higher sampling rates, in particular, would allow for increased ultra-wide band and microwave signal collection applications. Optical processing techniques are recognized as one of the ways to accomplish the multi-Gb/s sampling rates necessary for such applications. Many unique architectures have been investigated to take advantage of the higher sampling rates that are available [1-10]. Equation Chapter 1 Section 1

One method includes time stretching [1,2]. If a wideband received signal can be stretched in time before conversion, the required sampling rates can be relaxed. In order to do this in continuous time, however, parallel channels are needed to segment the time stretched signal. Another practice involves the use of Mach-Zehnder interferometers (MZI). These devices have a large bandwidth and an attractive periodic folding characteristic. MZIs are optical modulators in which the transmissivity (transfer function) of the device is periodic with respect to the applied voltage on the electrodes. This feature allows the modulator to serve as a folding circuit in an optical ADC where a sampling laser is used to sample the signal on the electrodes. The modulators can operate in parallel, as in [3], or in series. A series implementation is observed in [4] where a single-tapped MZI splits and recombines the light multiple times to achieve a 4-bit ADC. Other setups include working with phase modulation [5], pulsed lasers [6], and tunable lasers with Fiber-Bragg gratings [7]. Each has its advantages and drawbacks.

In this thesis, an optical three-channel folding ADC that uses a Robust Symmetrical Number System (RSNS) encoding was investigated [8,9]. The RSNS encoding results when the folding waveforms in each channel are amplitude-analyzed using a small number of comparators. The input signal is folded using three optical MZIs. One of the advantages of the RSNS is the increased resolution that the scheme can achieve (greater than 1-bit per interferometer) while using a minimal number of comparators. Another ad-

vantage of the RSNS is the inherent Gray-code properties in which the comparators used change state one at a time. A property of a Gray-code scheme is that if a bit-error occurs (for example, a comparator fails to change state from one code transition to the next), the resulting error is only one least significant bit. An RSNS encoding coupled with wide-band optical modulators and high-speed lasers would suggest an ADC design that has numerous advantages including high optical bandwidth, high efficiency, and a good degree of practicality. Implementing such a design was the focus of this thesis.

B. PRINCIPAL CONTRIBUTIONS

Several goals directed towards constructing a physical implementation of an electro-optical RSNS ADC were achieved. The main contribution included producing the three folding waveforms for a three-channel realization. These three waveforms were constructed through an all-optical infrastructure. Additionally, the sampling circuit was built and operates properly. A fully functional physical ADC infrastructure was not achieved due to the limitations of the DAQPad-6507, a data acquisition device that interfaces with the comparator circuits to provide data for analysis via a computer program called LabView. A different data acquisition device, preferably one with a hardware timing circuit, is required to collect the samples from the sampling circuit. Despite this drawback, much was accomplished.

A number of components were required for acquiring the necessary folding waveforms. Provided were a continuous laser, a 1x4 optical splitter, three circulators, three MZI modulators, three optical detectors complete with their own low-noise amplifiers, an oscilloscope, and two DC voltage sources. Before these components could function together as a circuit, many steps were involved. The first was to analyze the way in which the circulators were attached to the splitter and modulators. All of these were previously connected. However, in more than one instance, the connections had to be reconfigured so that the circuit could operate properly.

The next step involved replacing the two DC voltage sources as inputs to the Mach-Zehnder interferometers. In their place, a variable voltage source was acquired so that it was possible to observe if the optical infrastructure was working properly. The

voltage source that was used produced a triangle waveform. With this source, the voltage provided to the interferometers changed linearly with respect to time, a requirement if the folding waveforms are to be seen.

With the three folding waveforms established, the subsequent step was to manipulate the waveforms so that they complied with a three-channel RSNS. To do this, the periods and phases of the folding waveforms were set accordingly. This was accomplished through the use of three linear amplifiers and three coaxial cables.

The second part of the implementation dealt with the comparators within each channel required to sample the folding waveforms. A prepared circuit board with three comparator chips of four comparators each (twelve total) were provided initially. To effectively sample the folding waveforms, a method for setting the threshold voltages of the comparators was devised. LabView, a computer program by National Instruments, along with a DAQPad-6507, provided an efficient way to write a program to set the comparator threshold voltages. A series of digital code words had to be sent to the comparator circuit board through two 8-bit ports in the DAQPad. These digital code words activated a series of chip selects and comparator selects, as well as wrote an 8-bit reference word to each comparator.

After the program to setup the comparators was completed, another program was created to sample the comparator states in continuous time. This was also achieved through the DAQPad and LabView. However, the sampling rate maxed out at 1 kHz, several orders of magnitude short of where it was required to be for the whole ADC prototype implementation to be successful. Full completion of the ADC would consist of obtaining a faster data acquisition device and then reading samples into a data file for analyzing. If this were to happen, the advantages and practicality of an RSNS system supported by an optical infrastructure could be observed firsthand.

C. THESIS OUTLINE

Chapter II of this thesis is aimed at explaining the theory of the RSNS and clarifies the system properties before demonstrating how it was physically implemented.

Chapter III is an in-depth look at the physical components of the design and how they function together. A large part of Chapter III is dedicated to the interferometers and comparators used in the ADC.

Chapter IV reveals how the components in Chapter III are manipulated to produce the RSNS encoding. This chapter answers any questions about how the folding waveforms were generated and how the comparators serve to amplitude-analyze them.

The results, including the folding waveforms and those from LabView programs are displayed in Chapter V. Finally, a conclusion featuring the accomplishments and implications of this design will make up Chapter VI, including a detailed description of the equipment needed to complete the prototype.

II. ROBUST SYMMETRICAL NUMBER SYSTEM

This chapter describes the requirements of a RSNS encoding scheme. The theory behind the system also makes clear the advantages of an RSNS encoding.

Equation Section (Next)

A. INTRODUCTION

The Robust Symmetric Number System (RSNS) is a preprocessing method used by folding ADCs as proposed in [9]. An ADC that implements a RSNS scheme has a number of advantages over a typical Flash ADC. For one, an ADC using a RSNS architecture uses fewer comparators. Within the comparator network shown in the following block diagram (Figure 1), a total of twelve comparators are required to achieve an $n = 6$-bit resolution. A flash ADC, on the other hand, needs $2^n - 1$ comparators to realize a resolution of n bits. Figure 2 shows the configuration of a Flash ADC that has a 3-bit resolution. To come up with a 6-bit resolution, a flash ADC needs 63 comparators, compared to the RSNS requirement of 12.

The RSNS is an efficient system, however, it is not the most optimal. The most optimal system that can be implemented is the Optimum Symmetrical Number System (OSNS) [9]. An OSNS offers the greatest dynamic range for a given number of compara-

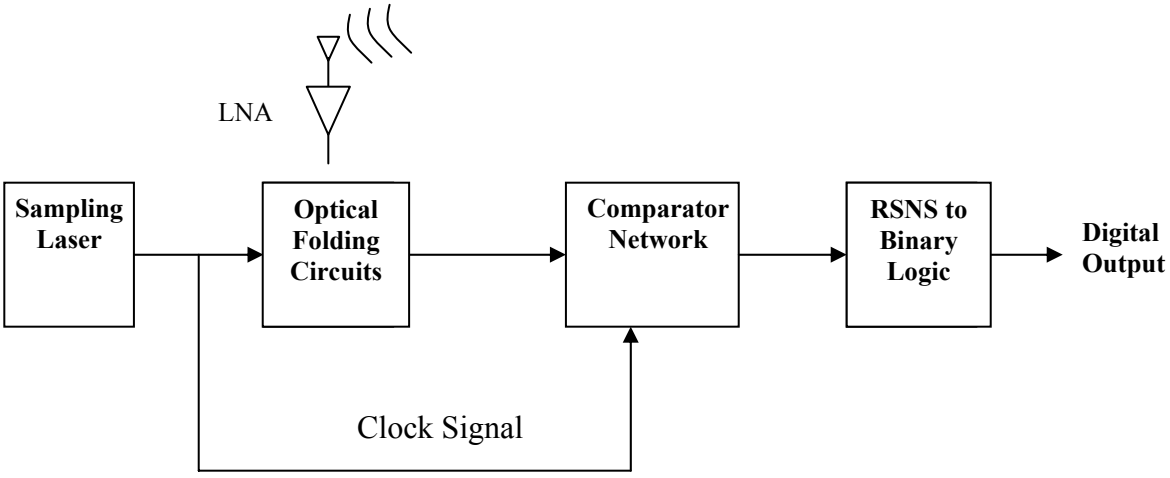

Figure 1. Block Diagram of ADC

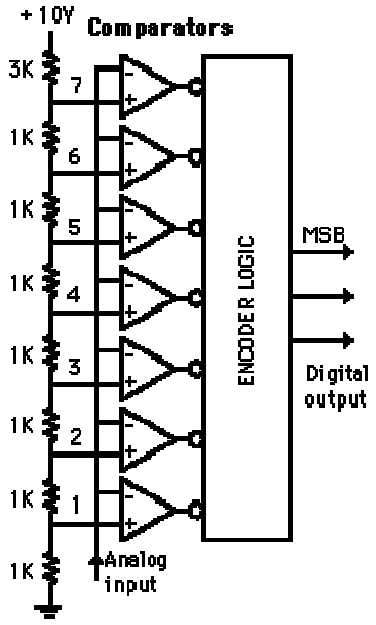

Figure 2. Typical Flash ADC Design with 3-Bit Resolution (From hyperphysics.phy-astr.gsu.edu)

tors. As a preprocessing technique, though, there are drawbacks to choosing this system. The digital words corresponding to analog input values in an OSNS do not follow a Gray-code pattern. This is due to the fact that comparators are required to change states simultaneously at each code transition as the analog input changes in magnitude. Without the high degree of precision necessary to have this happen, errors are more likely. In addition to the difficulty of providing such precision, the absence of a digital Gray-code sequence means that a one-bit encoding error will result in a disproportionately large conversion error. [9]

ADCs featuring the RSNS, though, not only are more efficient than most ADC architectures but offer a Gray-code digital output pattern as well. Since the comparators need only change states one at a time, the digital words describing sequential analog inputs change by only one bit at a time. Thus, the RSNS is most robust against encoding errors. Though an ADC design employing an RSNS system is not the most optimal, it remains both efficient and practical. [9]

1. RSNS Theory

The following describes how to set up a RSNS. RSNS architectures may have any number of *N*-parallel channels, but in this implementation $N = 3$. In an *N*-channel RSNS, there exists *N* separate symmetric and periodic folding waveforms. These waveforms are based on a row vector x_{m1} through x_{mN} where m_1 through m_N are all positive integers and relatively prime with one another. The row vector, x_{m1}, is defined as:

$$x_{m1} = [0, 1, 2, ..., m_1 - 1, m_1, m_1 - 1, ..., 2, 1]. \tag{2.1}$$

Each of the *N* channels has its own modulus, *m*, and is based on the row vector, x_{mi} where *i* represents the i^{th} channel. The i^{th} channel's row vector can be further described by repeating each element in its row vector *N* times. The resulting row vector for channel *i* is as follows:

$$x_{mi} = [0, 0, ..., 0, 0, 1, 1, ..., 1, 1, ..., m_i, m_i, ..., m_i, m_i, ..., 1, 1, ..., 1, 1]. \tag{2.2}$$

If this row vector were repeated endlessly on both sides and made periodic, then it would be an accurate model for the folding waveform present at the i^{th} channel. The period of the i^{th} channel row vector is given by:

$$P_i = 2m_i N, \tag{2.3}$$

where *N* is the number of channels. Figure 3 portrays how each of the three channels in this ADC implementation is related to their respective row vectors. Notice that a modulus-*m* channel has *m* threshold levels that amplitude-analyze the folding waveforms. Also note that each integer within the row vectors represents the number of comparators in the ON state. That is, the voltage level of the waveform, in comparison to the thresholds, determines the integers within the channel's corresponding row vector. For instance, the modulus-3 channel starts with the amplitude of the waveform in between comparator threshold values T1 and T2. In the modulus-3 row vector at the bottom of the figure, this corresponds to a row element of 1. Moving to the right along the folding waveform, the amplitude drops below T1, resulting in the row element changing to a 0. Continuing in this fashion will show that the row vector accurately models the folding waveform. There

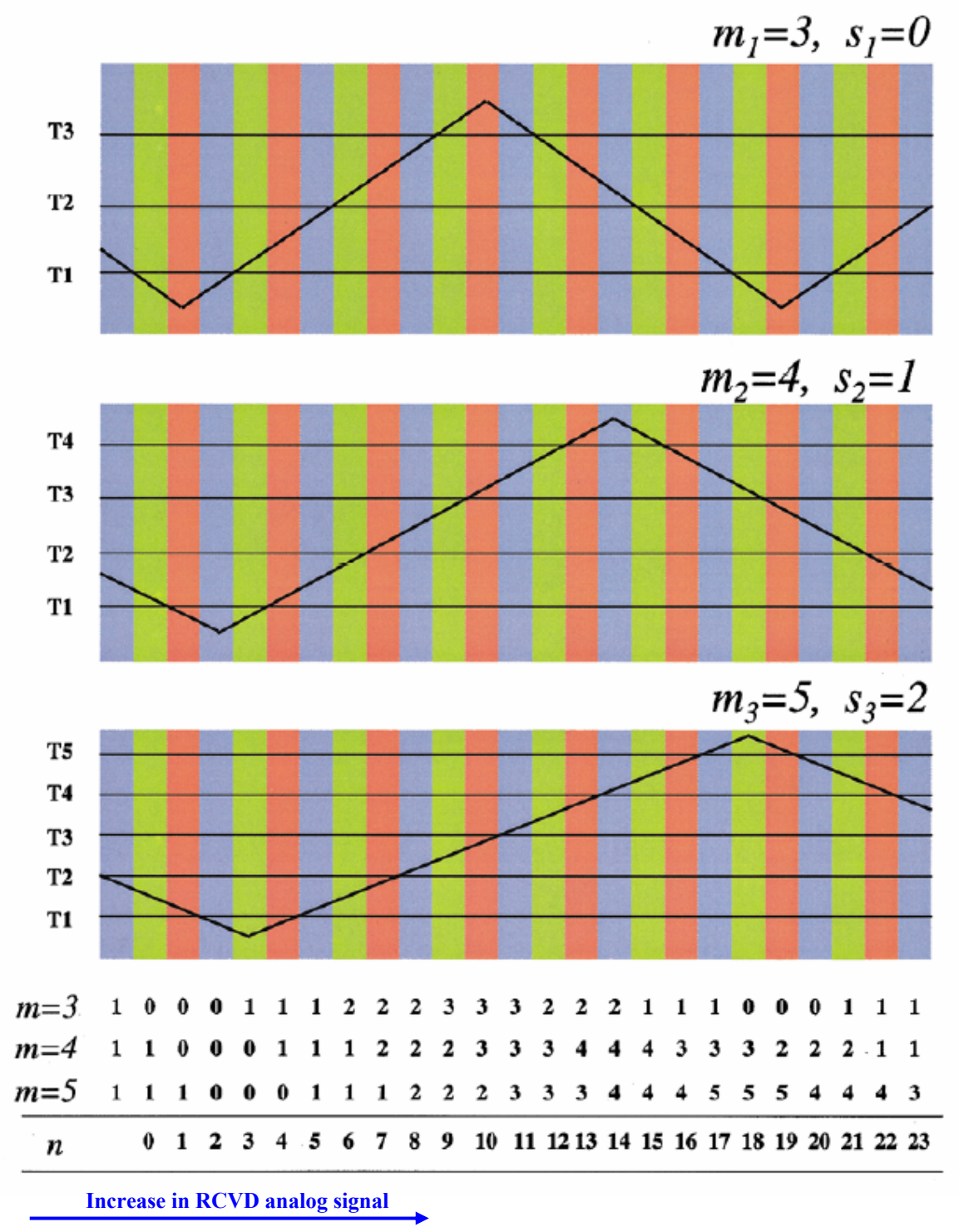

Figure 3. Folding Waveforms of RSNS with Corresponding Row Vectors (From [9].)

are many characteristics of Figure 3 worth noting. For one, these three channels contain row vectors that, when taken together, produce a Gray-code pattern from one column of row vector elements to the next. That is, only one comparator (row element) changes state during any code transition. This is accomplished by setting the period and phase of each waveform. The phase shift, which is more apparent in the first few transitions of Figure 3, is essential to maintaining the Gray-code sequence. The folding periods of the three waveforms also have the following relationship:

$$P_1 = \frac{3}{4}P_2, \quad P_2 = \frac{4}{5}P_3. \tag{2.4}$$

In terms of the voltage, V_π, the folding period of each folding waveform is:

$$P_j[\mathrm{V}] = \frac{2V_\pi}{2mjN} = \frac{V_\pi}{3mj}, \tag{2.5}$$

where V_π is the amount of voltage required to drive the modulator output from a maximum to a minimum or vice-versa.

The dynamic range, $\hat{M}$, of the RSNS is defined as the maximum range of distinctly unique column vectors throughout the system. The equation determining the dynamic range is given by [9]:

$$\hat{M}_{RSNS} = \frac{3}{2}m_1^2 + \frac{15}{2}m_1 + 7 \tag{2.6}$$

where m_1 is the modulus of the first channel.

To better explain the dynamic range of a RSNS encoding, take, for example, in Figure 3, the digital word at element $n = 2$ that is 000. The next instance of this word is at element $n = 29$ (not shown). Thus, the sequence goes through a range of 28 elements before repeating the digital word. If these three row vectors were extended out indefinitely, the Gray-code digital sequence would be shown to be periodic. As a result, there exist more vectors that contain distinctly unique vectors as well. The length of the vector with the greatest range is considered the dynamic range. Table 1 is a table displaying the

ranges of digital words that go without a repetition. The table makes apparent that the dynamic range of $\hat{M} = 43$ for this three-channel RSNS, which starts at $n = 61$ and ends at $n = 103$.

Beginning Point Index	Ending Point Index	Total Length
2	29	28
7	30	24
8	41	34
13	51	39
23	52	30
24	57	34
41	65	25
61	103	43

Table 1. Beginning, End, and Length of Code Sequences Without Repetition (From [9].)

Referring back to Figure 3, observe the phase shifts of the three waveforms. The modulus-4 waveform is lagging the modulus-3 waveform by one code width at $n = 0$. The waveform with modulus-5 is lagging the modulus-3 waveform by two code widths. It so happens that no matter how these three waveforms are shifted relative to each other, the dynamic range of the system remains constant ($\hat{M} = 43$). This is assuming that the shifts are not in multiples of three, which would destroy the Gray-code property of the system. The work for this is shown in [9].

In summary, the theory behind the RSNS architecture and its advantages has been addressed. The efficiency of the system comes from the three parallel folding waveforms and the few number of comparators used in the analog-to-digital conversion process. At the same time, the scheme is practical in that the columns of the three row elements maintain a Gray-code sequence for any code transition point. The RSNS ADC hardware implementation is discussed in the next two chapters. The circuit block-diagram, along with the component details, is also presented.

III. PHYSICAL CIRCUIT DESIGN

The physical design of the ADC employs optical components as well as electrical components. This provides an avenue for the development of wideband analog-to-digital applications. An overall circuit design is illustrated in this chapter along with a description of the devices used.

Equation Section (Next)

A. BLOCK DIAGRAM

Figure 4 shows a detailed schematic of the RSNS ADC architecture. A received analog signal (acquired through an antenna) is amplified using an LNA, sampled, and converted into a binary format. The sampling of the analog signal of interest at each modulator is accomplished using an optical pulse from the laser. The optical pulse is

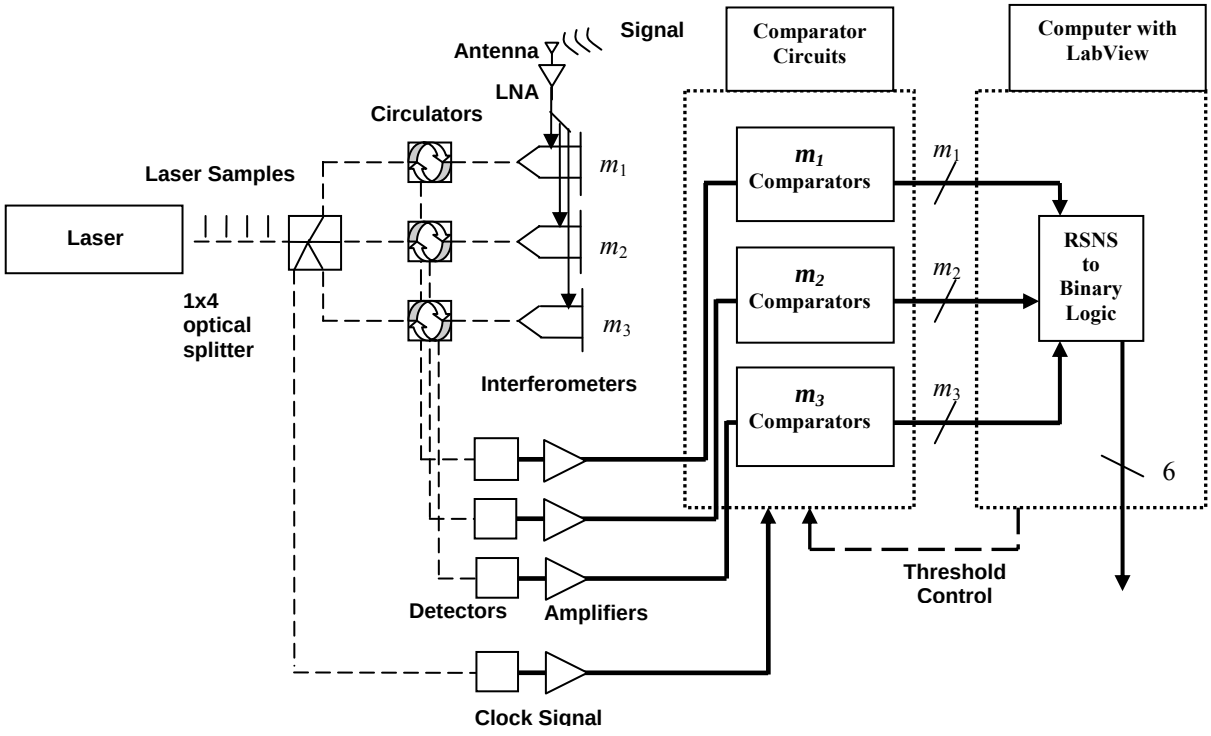

Figure 4. Circuit Block Diagram

divided by a 1x4 optical splitter and sent to three $LiNbO_3$ MZIs that amplitude modulate the pulse as a function of the analog antenna signal. Three modulated optical pulses are then detected, amplified, and amplitude-analyzed by three small groups of comparators. Each comparator consists of an amplifier and a latch. The amplifier amplifies the "difference" between the amplitude modulated pulse and the matching threshold voltage. The latch registers the two-state signal at the comparator output. Every bank of comparators generates its own set of outputs, which are combined in a logic block or read-only memory (ROM). The logic block then derives the resulting binary words that represent the digitized analog voltage and does so with a six-bit resolution. The following sections describe each RSNS ADC component in more detail.

1. Laser

The laser used in this architecture was a BCP 400 laser shown here in Figure 5. The yellow cabled optical fiber connected to the laser at the right carries a beam of light with a wavelength of 1310 nm. To obtain the laser pulses, the BCP can be triggered or the continuous wave light can be amplitude modulated externally. In this thesis however, neither of these methods was used. Instead, the laser provided a continuous-wave signal. Optical light, in the place of light pulses, then traveled through the fiber and arrive at a 1x4 optical splitter.

Figure 5. BCP 400 Laser Used as Input to Splitter

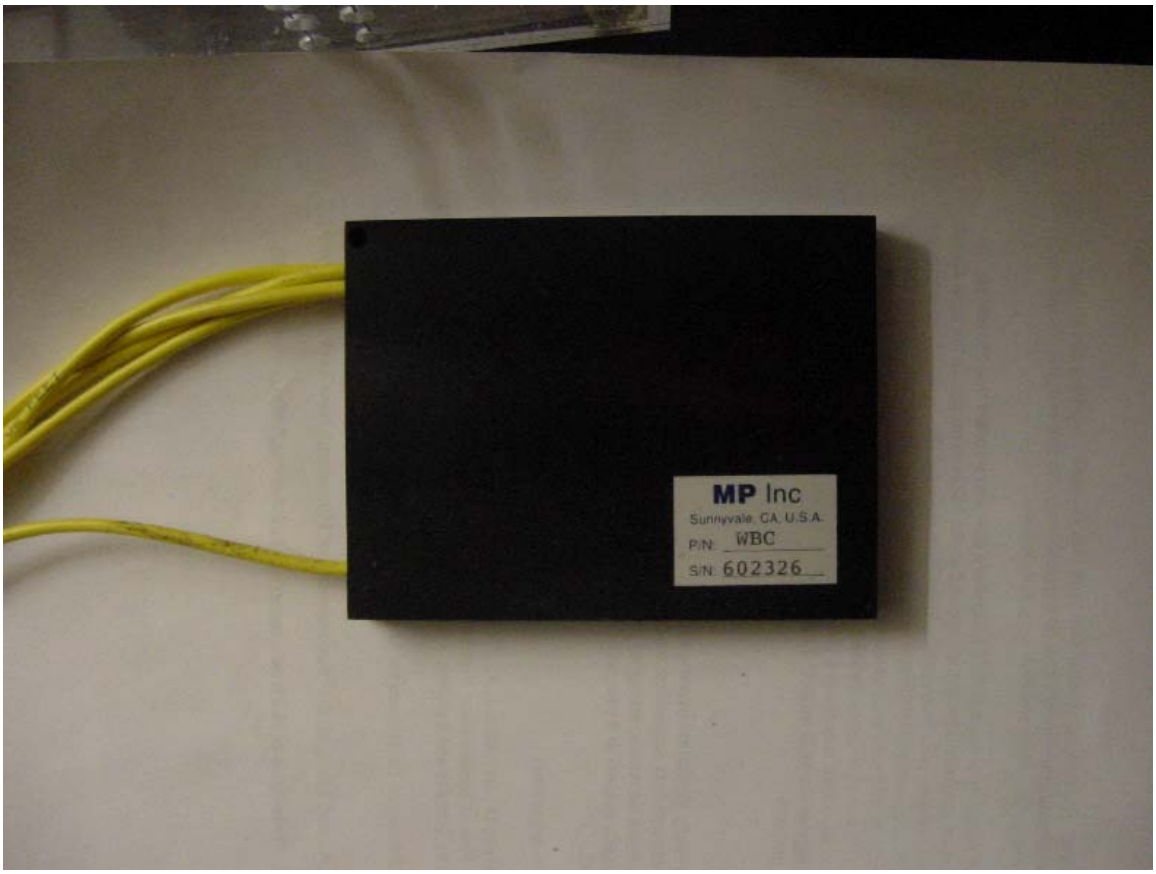

Figure 6. A 1x4 Optical Splitter

2. Optical Splitter

Figure 6 displays the 1x4 splitter used in the ADC architecture. It has one input and four outputs. In the figure, there is one input fiber to the device. The fiber is seen at the bottom of the figure and carries the light supplied by the laser in Figure 5. Ideally, the splitter takes an optical signal with power, P, and outputs four identical channels each with an optical power of $P/4$. Considering any losses however, the four output channels will have a power level of less than $P/4$. Of the four channels created by the splitter, only three are needed for sampling. This is due to the fact that the RSNS architecture used in this design only uses three channels. The fourth output may be used as a clock to register the system.

3. Circulators

The block diagram in Figure 4 shows that the optical pulses generated by the laser and split by the splitter enter three circulators before being input to the MZIs.

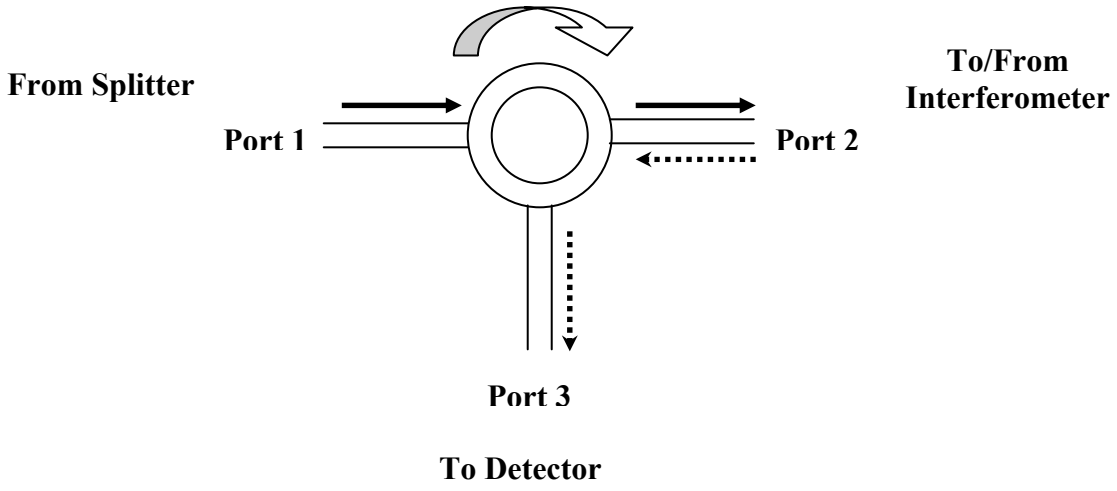

Figure 7. Three Port Optical Circulator

The interferometers themselves only have one port. Thus, separating what goes in through the port from what comes out is necessary. Circulators are essential devices in this architecture because they separate the inputs to the interferometers from the outputs.

The circulators used in the ADC architecture are three-port devices as shown in Figure 7. In this device, a signal arriving at a given port will enter the circulator and leave at the next port. For example, an optical signal entering the circulator at port 1 will propagate around the circulator and exit at port 2. A signal arriving at port 2 will be output at port 3. A typical circulator will also relay a signal arriving at port 3 and output it at port 1.

In the context of the ADC, port 1 of each circulator receives one of the channels from the laser through the 1x4 splitter. The light exits the circulator at port 2, and is sent to the interferometer. After the light is modulated within the interferometer, the signal re-enters port 2 of the circulator. Beginning at port 2, the modulated light signal exits the circulator at port 3, having been separated from the un-modulated light and sent to the detector.

4. Interferometers

A MZI, shown in Figure 8, operates by way of the Pockels effect, a characteristic of $LiNbO_3$ that causes the index of refraction, n, of the material in the guide to change based on the intensity of the electric field through it. If the index of refraction of $LiNbO_3$ without any electric field present is n_o then the relationship between n, and an electric field, E, is as follows:

$$n(E) \approx n_o - \frac{1}{2} r n_o^3 E. \tag{3.1}$$

where r is the electro-optical constant for the material. The ability to change the index of refraction allows the user to affect the speed of signal propagation through the device. The speed of propagation through an optical device is equal to c/n (c being the speed of light). [10]

After receiving light from port 2 of the circulator, the interferometer splits the light into two identical beams which travel along the channels until being reflected by a reflective surface at the opposite side of the device. The two beams then travel in the reverse direction through the same channels and are recombined before exiting the device. During the period of time the light is propagating through the two channels, the speed at which it propagates will change based on the applied voltage, $V(t)$, to the device. Since the electric field generated by the voltage is opposite in polarity for the two channels,

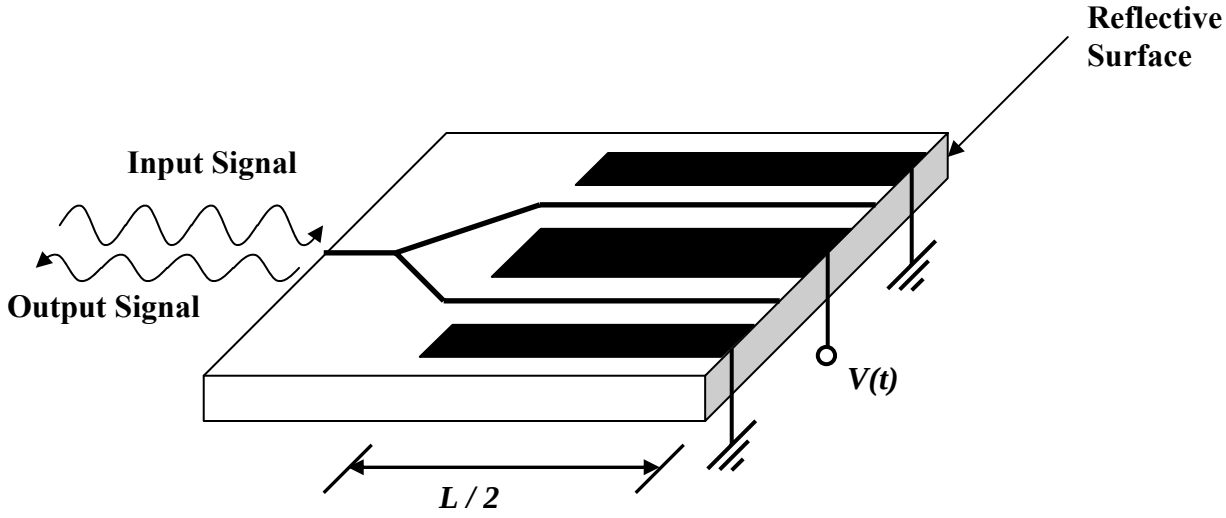

Figure 8. Reflective Mach-Zehnder Interferometer Design

a relative phase shift is introduced between the two beams of light as they propagate through a total distance of L. The total phase shift between the two beams determines how the beams will interfere when being combined at the output. The transmittance of a Mach-Zehnder interferometer is given by:

$$T(V) = \cos^2\left(\frac{\varphi_o}{2} - \frac{\pi V}{2V_\pi}\right), \tag{3.2}$$

where V_π is the change in voltage that will adjust the relative phase of the two optical beams by 180 degrees and φ_o is any static phase shift present from, for example, a difference in length between the two channels [10]. If the total phase difference is 180 degrees, then the beams will destructively interfere and cancel each other out. Figure 9 shows the plot of the transmittance relative to $V(t)$. Note the difference in $V(t)$ between peak and adjacent null. A change in voltage that shifts the relative phase by 180 degrees, is known

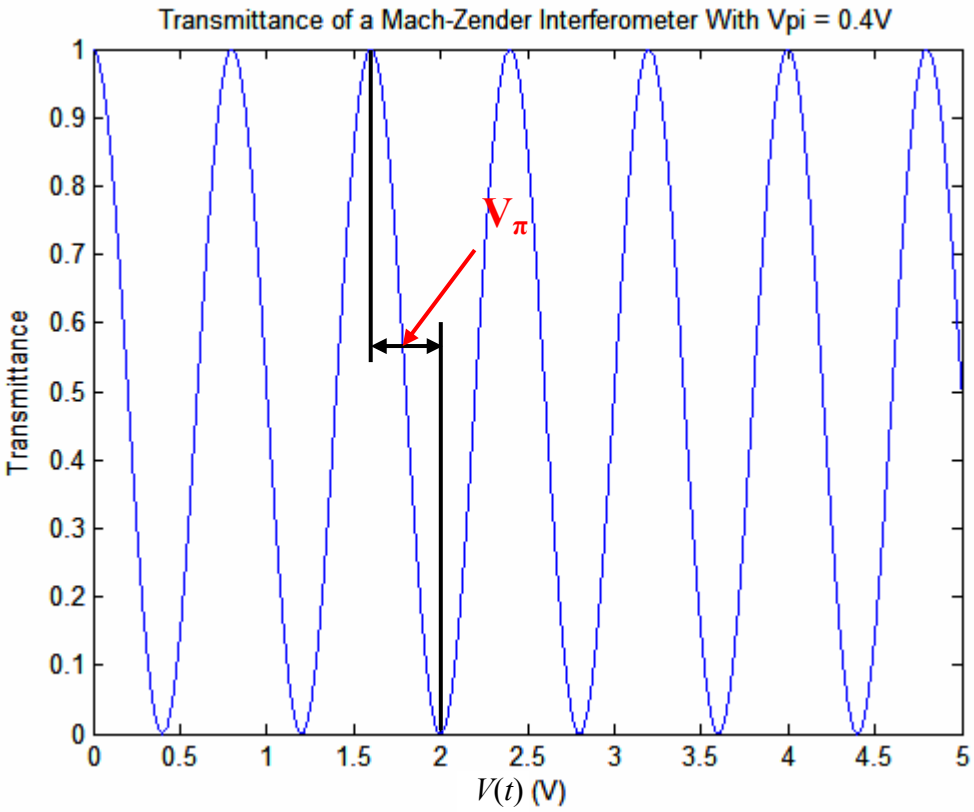

Figure 9. Theoretical Transmittance of Interferometer Vs. Analog Modulating Voltage

as V_π. The value of V_π can vary from interferometer to interferometer. V_π depends on the geometry of the interferometer and has the relationship,

$$V_\pi[\mathrm{V}] = \frac{d\lambda}{Lrn^3}, \tag{3.3}$$

where d is equal to the channel width, λ represents the wavelength of the light, L is the total length of the channel, and n is the index of refraction of the material. For the interferometers used in the ADC, each has a $V_\pi \cong 0.4$ V. [10]

The outputs of the interferometers enter the circulators at port 2 and exit at port 3. From there, the modulated optical signal is received by the three optical detectors. Figure 10 is a photo of the components for one optical channel. From the splitter, light is guided through a circulator and an interferometer. There are three setups identical to the one shown in Figure 10.

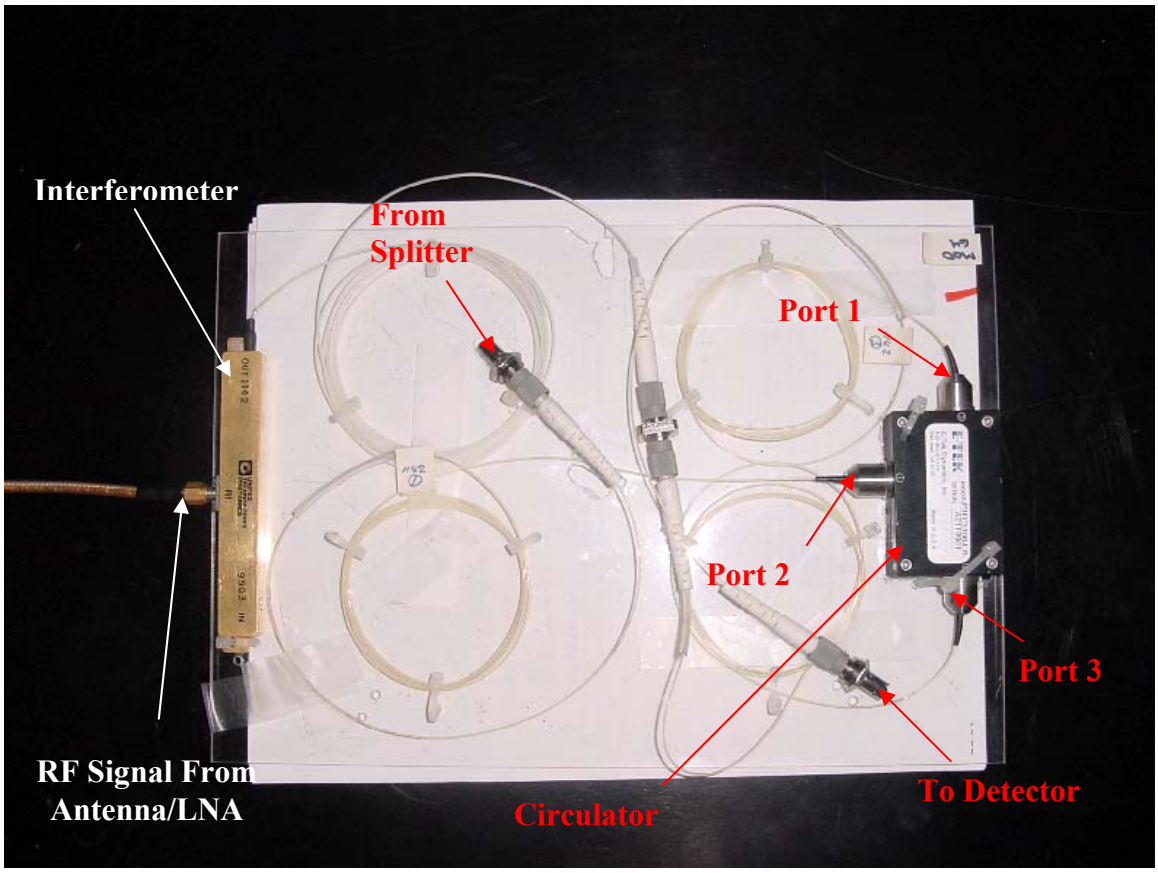

Figure 10. Optical Circuit for One RSNS Channel

In order to complete the analog-to-digital conversion, samples of the RF signal must be taken by each of the three optical channels. One of the advantages of this optical architecture is that it can efficiently couple the wideband RF signal into the optical domain for processing. The received signal bandwidth that can be analyzed, however, is limited by the sampling rate of the laser, since the sampling rate must be at least twice the maximum frequency in the signal.

5. Detectors

Three detectors are used in the ADC circuit to convert the three optical signals to electrical signals. A BCP 310A Optical to Electrical converter is shown in Figure 11 and contains both a detector and an amplifier. The fiber cable from port 3 of the circulator for a given channel is shown at the very right of the converter. From there, the signal is changed into an electrical signal and sent to the linear amplifier displayed in the middle of the device in Figure 11.

Figure 11. BCP 310A Optical to Electrical Converter

Referring back to the block diagram in Figure 4, one can see that the converted and amplified signal is sent to three separate comparator banks, one for each channel. The comparators perform the amplitude analysis of the three electrical signals containing a sample of the RF signal.

6. Comparators

All three channels measure the signal's amplitude using a bank of comparators. A symbol representing a comparator is shown in Figure 12. The comparator is made up of a differential amplifier followed by a latch. The comparator compares a voltage, $V_{SIG}(t)$, to some reference voltage, V_{REF}. If V_{SIG}(t) is higher than V_{REF} when the clock goes high at time, t, then the comparator will output a high voltage of $+V_{CC}$. Conversely, the comparator will output a 0 if $V_{SIG}(t)$ is less than V_{REF} at time, t. In order to measure the amplitude of $V_{SIG}(t)$, multiple comparators are used in parallel. A single comparator can describe the amplitude of a signal with a resolution of 1 bit.

If three comparators are used, a resolution of 2 bits can be achieved. Figure 13 displays three comparators set up much like a Flash ADC. If the range of amplitudes that $V_{SIG}(t)$ could realize is from 0 to +REF volts, then three comparators could split that range into quarters. With reference voltages of 0.25*REF ,0.50* REF , and 0.75* REF the comparator states will confirm which quarter of the range, 0 to +REF volts, the amplitude of $V_{SIG}(t)$ occupies.

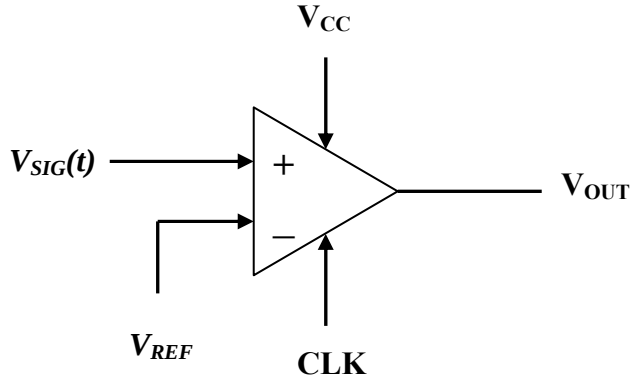

Figure 12. A Comparator

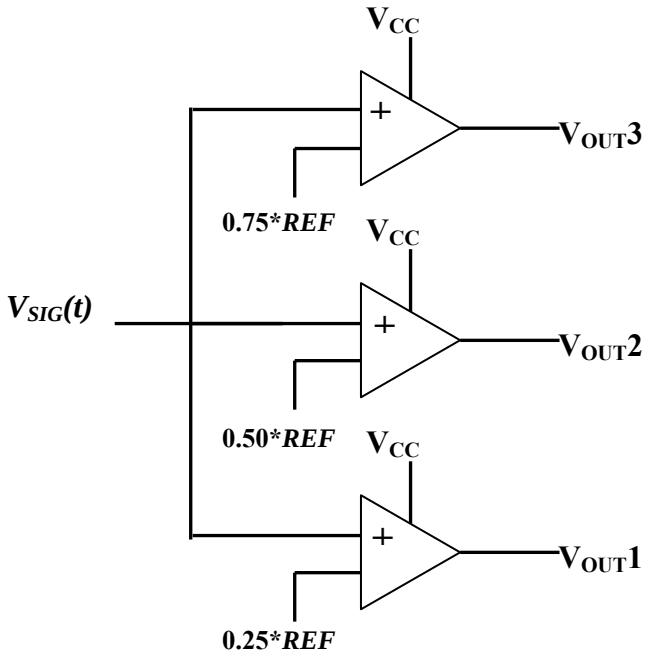

Figure 13. Comparator Bank for Modulus-3 Channel

The comparator bank for the Modulus-3 channel has three comparators, with three reference voltages shown in Figure 13. The thermometer code for this example is shown in Table 2. For the Modulus-4 and Modulus-5 channels, the number of comparators in the banks is four and five with the channels splitting the range of 0 to +REF volts into fifths and sixths, respectively. An important difference between the uniformly spaced reference voltages in Figure 13 and the ideal reference voltages that should be applied in the three-channel RSNS ADC is that the folding waveform of the ADC is not a perfect triangle wave. The waveforms resulting from the MZIs are cosine squared functions. In order to divide this folding waveform into least significant bits of equal width, the threshold voltages cannot be uniformly spaced. Threshold values of 0.067*REF, 0.5*REF, and 0.933*REF volts, are required to obtain the equal widths for the least significant bits in the modulus-3 channel. For the sake of simplicity, uniform spacing, shown in Figure 13 for the modulus-3 channel was used to test the functionality of the comparator banks.

Adding the number of comparators needed for the three channels yields a total of twelve. To accommodate this number, the comparator bank requires three four-

Thermometer Code

Amplitude of $V_{sig}(t)$	Comparator states ($V_{out}3$, $V_{out}2$, $V_{out}1$)
between 0.75**REF* and *REF*	111
between 0.50**REF* and 0.75**REF*	011
between 0.25**REF* and 0.50**REF*	001
between 0 and 0.25**REF*	000

Table 2. Comparator States Given a Received Voltage

comparator MAX516 devices. The device has 24 pins in a dual-inline package. Within the device, four different inputs are compared to four programmed 8-bit reference voltages and yield four separate outputs. Each of the four comparators is completely independent of the others as far as input, reference, and output voltage levels.

Figure 14 shows the pin diagram for the MAX516 quad-comparator. Pins 3 (V_{CC}) and 22 (V_{DD}) supply power to the device. The voltage levels supplied to these pins range from 5 V to 15 V, but are typically equal. The ground for the current is at pin 6. The analog inputs for the four comparators are labeled AIN0, AIN1, AIN2, and AIN3. $V_{SIG}(t)$ can be input to any number of these inputs by tying the pins together externally.

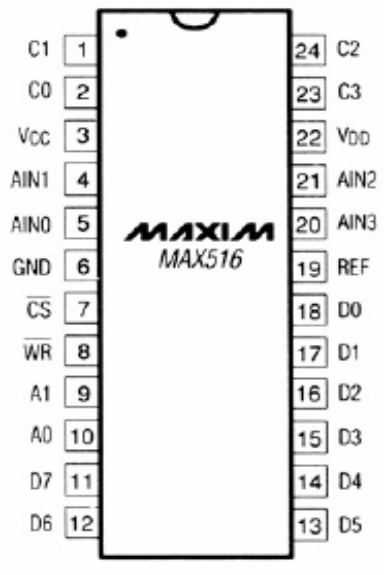

Figure 14. MAX 516 Pin Diagram

The MAX516 device allows the reference voltages for the four comparators to be programmed independently. Each of the comparators has its own digital-to-analog converter (DAC). Writing an 8-bit word describing the threshold voltage for a given comparator requires that it be loaded to that comparator's DAC. To accomplish this, there are many steps. The first step involves choosing the 8-bit word to load to the DAC. For a reference voltage of V_{REF}, an 8-bit word with a base-10 value of X is required according to the equation:

$$V_{REF}[\mathrm{V}] = +\mathrm{REF} * \left(\frac{X}{256} \right). \tag{3.4}$$

The 8-bit word corresponding to X is loaded at pins 11 through 18. Pin 11 (D7) represents the most significant bit of the word while pin 18 (D0), the least.

The full range of amplitudes that the comparators can effectively amplitude-analyze is given by +REF. This value is set using pin 19 (REF). A comparator's DAC is selected through pins 9 (A0) and 10 (A1). A combination of the digital states at pins 9 and 10 results in the ability to write to one of four comparators. Table 3 displays the table for selecting a DAC. In this thesis, three MAX516 devices were used. A chip select at pin 7 was used to differentiate between the three. To select a device for writing of a reference voltage to one of its four DACs, a low of 0 V must be sent to pin 7 on that device.

Once the device is selected via pin 7, the comparators DAC selected via pins 9 and 10, the 8-bit word chosen for pins 11 through 18, and the range, REF, of the reference voltages set through pin 19, a rising edge must be seen on pin 8 (WR). This loads the reference voltage into the DAC of a given comparator [See Appendix].

A1	A0	DAC selected
0	0	DAC0
0	1	DAC1
1	0	DAC2
1	1	DAC3

Table 3. Selecting a DAC Using A0 and A1

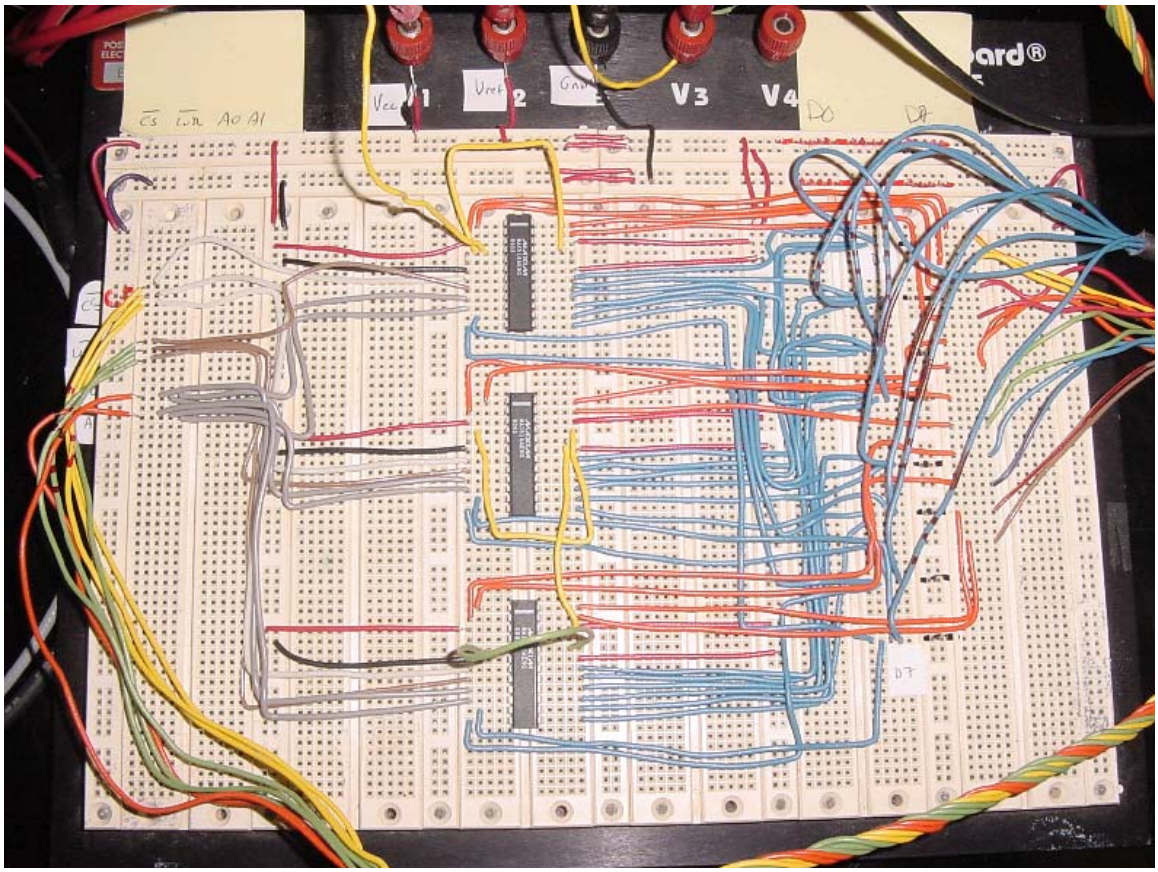

Figure 15. Comparator Banks for All Three RSNS Channels

The fully wired comparator circuit is displayed in Figure 15. In this figure, the top MAX516 chip is used in conjunction with the Modulus-4 channel. The bottom two chips are used for the Modulus-3 and Modulus-5 channel. This setup is the simplest as far as keeping the channels spatially separated.

A computer program called LabView 7.1 from National Instruments was used to set the reference voltages for all twelve comparators. The program will be described in detail in a later chapter.

Chapter IV describes how the tools and devices just discussed are integrated to accomplish the RSNS encoding in Chapter II. Equation Section (Next)

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IV. RSNS IMPLEMENTATION

The Robust Symmetric Number System represents a practical and efficient pre-processing scheme for ADCs. The hardware to build the ADC architecture in this thesis was presented in the last chapter. In this chapter, the hardware configuration necessary to develop a RSNS ADC encoding is presented.

A. FOLDING WAVEFORM PERIODS

Applying a three-channel RSNS to an ADC requires that the outputs of the comparator banks shown in the block diagram in Figure 16 produce a Gray-code sequence as the signal received through the interferometers increases or decreases in magnitude. Thus, three folding waveforms with different periods and shifts must be produced by the optical folding circuits.

A single channel acquires its folding property from the MZI. Looking back at the transmittance of an interferometer, it becomes apparent that as the received signal (V_{in} in Figure 9) steadily increases, the optical signal's intensity at the output rises and falls with a folding period of $2V_{\pi}$.

The three-channel RSNS demands three folding waveforms with periods related

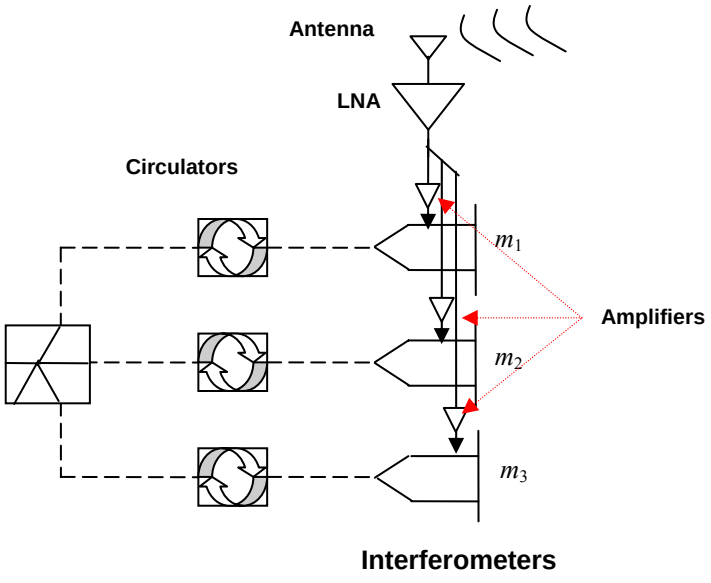

Figure 16. Placement of Amplifiers in Circuit Diagram

to each other by Equation 2.4. All of the interferometers used in this architecture are identical designs. The V_π values for all three devices $\cong 0.4\text{V}$. External devices are called upon to provide the correct folding periods for each MZI. The devices are linear amplifiers that scale the received signal being input to the interferometer. Figure 16 shows where amplifiers are added in the block diagram.

The concept behind adding three amplifiers to modify the periods of the folding waveforms is better illustrated in the three graphs of Figure 17. A linear increase in the received signal voltage with respect to time is demonstrated in the three graphs. Each of these graphs has a different rate of voltage increase. This is due to the amplification of the received signals before being input to the three interferometers. Different slopes are the result of different amplification gains. Figure 18 reiterates the transmittance

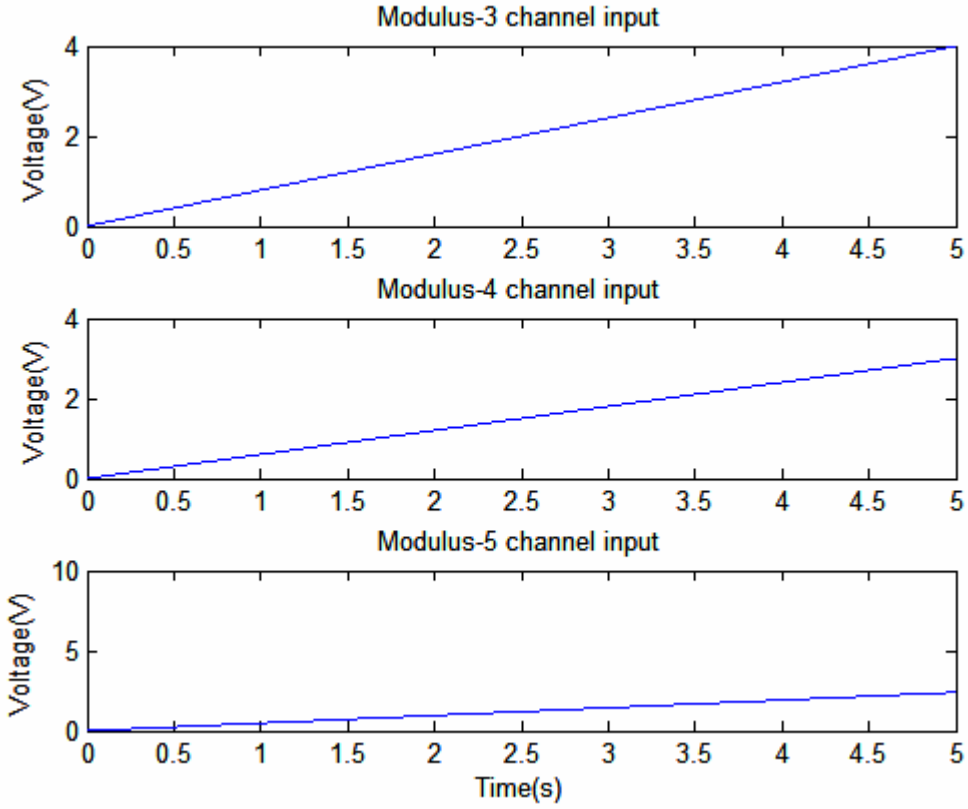

Figure 17. Analog Received Signals with Use of Three Amplifiers of Different Gains

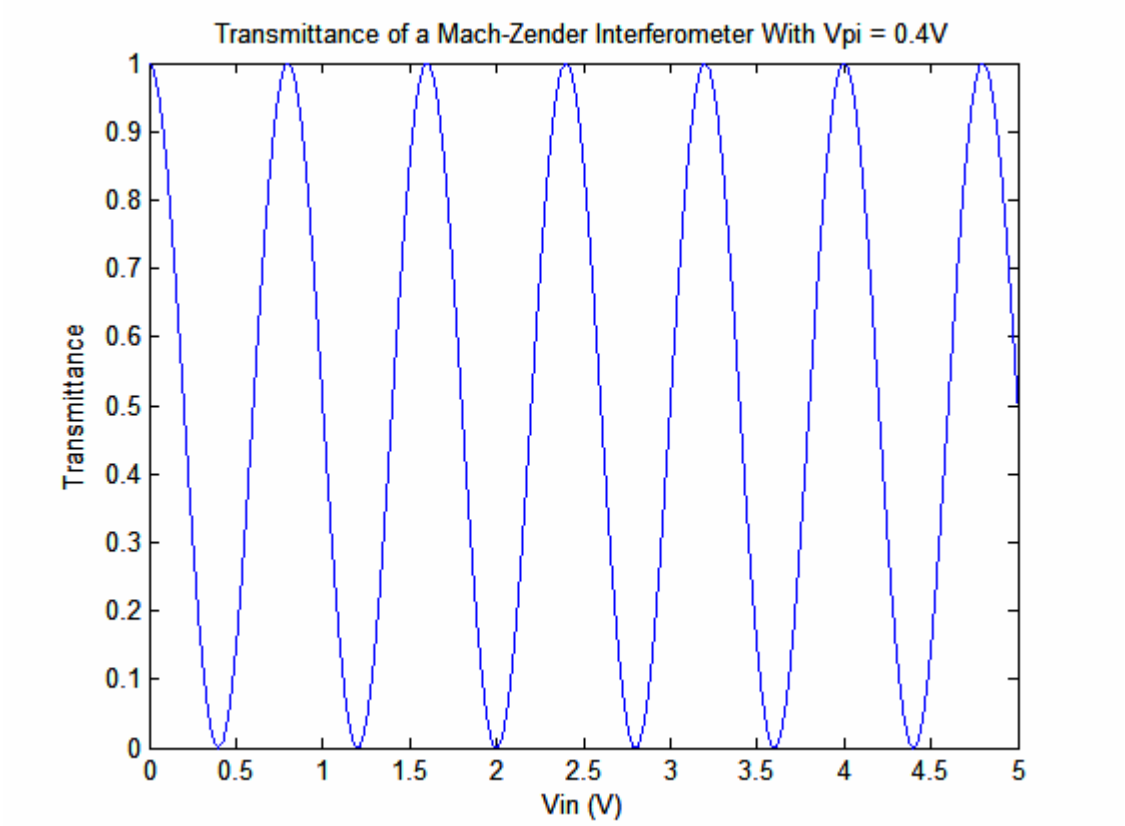

Figure 18. Theoretical Mach-Zehnder Interferometer Transmittance

characteristic of the interferometer with $V_\pi = 0.4\text{V}$. Feeding the signal inputs of the three graphs into the V_{in} axis of the transmittance graph yields three folding waveforms of different periods. Much like the relationship of the waveform periods in Equation 2.4, the gains of the three respective amplifiers (in V/V) must be related to each other in the following way:

$$G_1 = \frac{4}{3}G_2, \quad G_2 = \frac{5}{4}G_3. \tag{4.1}$$

Notice that the gains are inversely proportional to the periods of the waveforms. This is due to the fact that as the slope of an input voltage increases, the period of the corresponding interferometer output decreases. Figure 19 displays the results of this concept.

Given the received signal inputs presented in Figure 17, the three graphs of Figure 19 represent the matching interferometer outputs. The periods of the folding

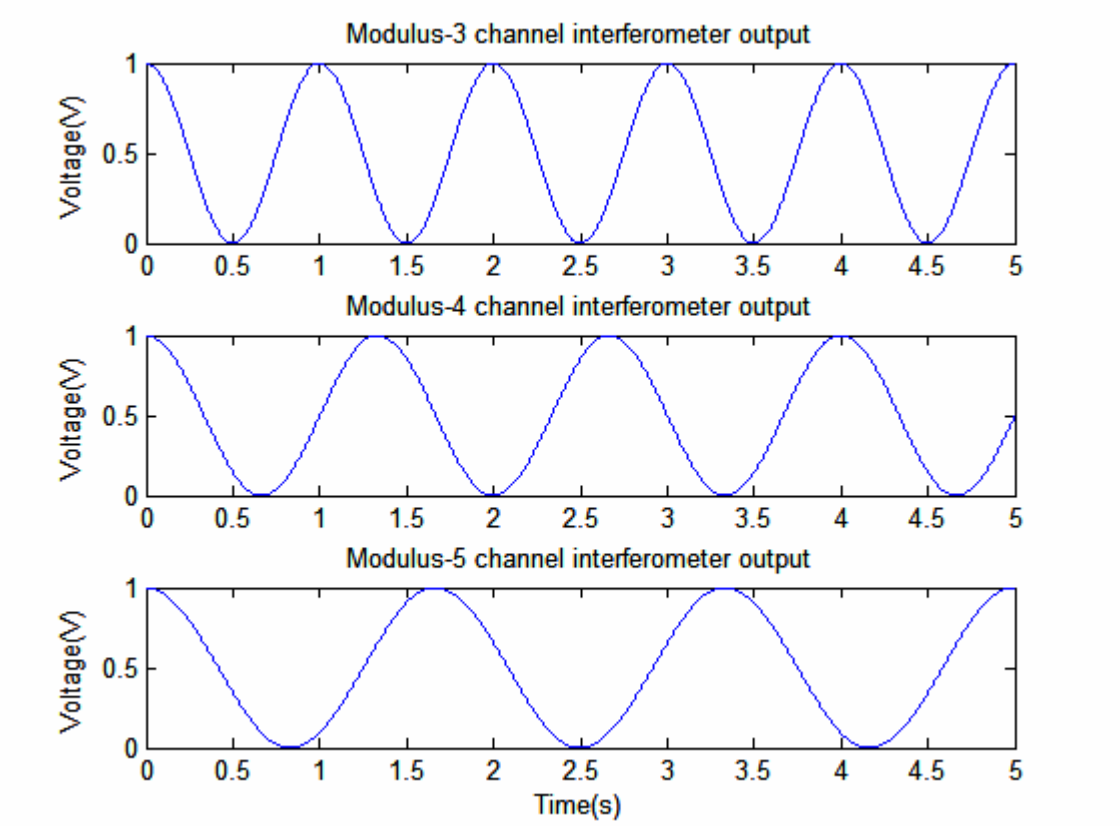

Figure 19. Modulator Outputs Given the Inputs in Figure 17

waveforms are in line with the requirements of the RSNS implementation. A phase shift is still lacking in these output waveforms though.

B. FOLDING WAVEFORM PHASE SHIFTS

Recall that a shift between the three folding waveforms is central to maintaining a gray code sequence in that the row vectors change the value of subsequent elements one at time. No set of amplifier gain values can implement this shift. Gain modifies how quickly the transmittance of the interferometer cycles through its period, thus, affecting the output period. There are two methods for creating this shift.

The first is with a DC offset that is applied to the interferometer inputs after amplification. Values of DC offset for each of the three channels is dictated by the period of the waveforms. Figure 20 revisits Figure 3 and shows the modulus-3 and modulus-4

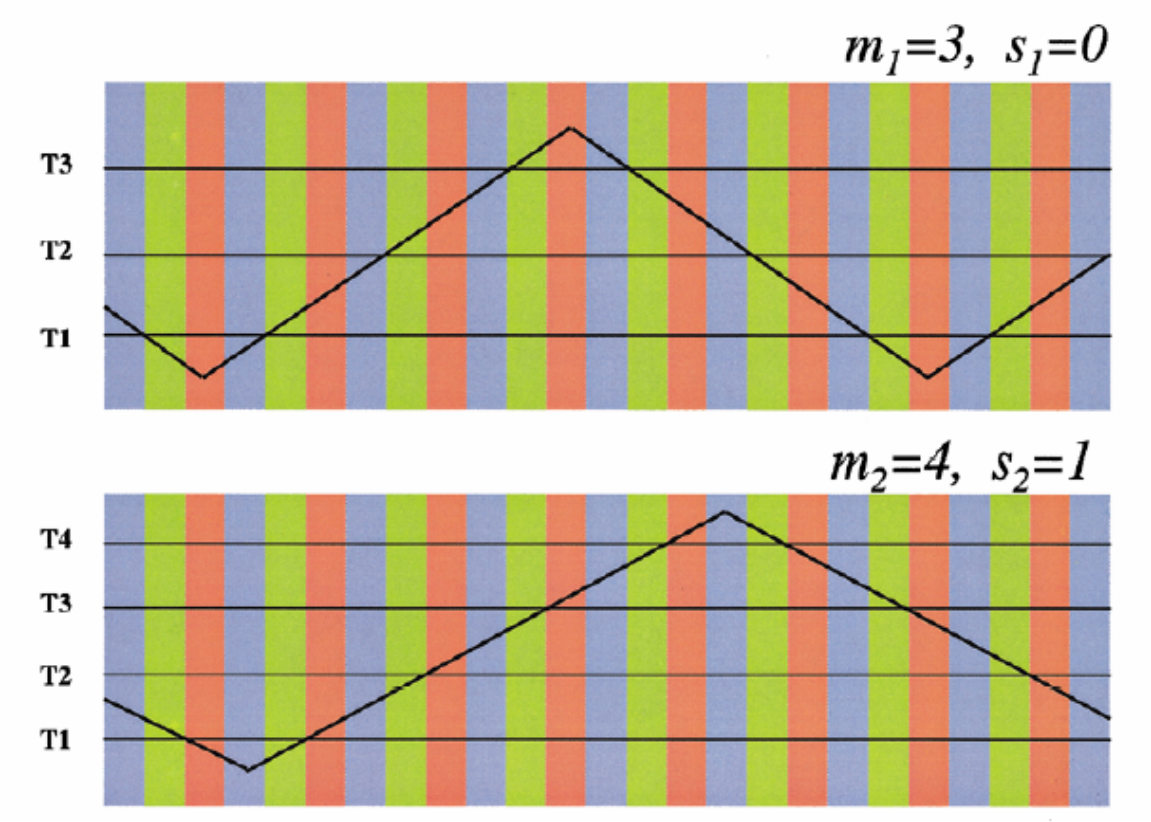

Figure 20. RSNS Modulus-3 and Modulus-4 Channels (From [9].)

waveforms. Equation 2.3 accurately describes the periods of these two waveforms. Observe that P_1 is equal to 18 divisions ($m_i = 3$, $N = 3$), or 18 digital word transitions. Shifting a waveform one division farther to the right requires that one do so by an amount that is one-eighteenth the size of the period of the modulus-3 waveform or one twenty-fourth of the period ($m_i = 4$, $N = 3$) of the modulus-4 waveform. With this in mind, the amount of DC offset needed for each interferometer input becomes clear. If the hypothetical value of the period of the modulus-3 waveform was 0.72V, which would also be the value, $2V_\pi$, then the DC offset needed to shift any of the three waveforms by one digital word in the RSNS is one eighteenth of that value, or 0.04V.

A second method is also available to shift the folding waveforms. This method works by introducing time delays to the received signals. The time delays are introduced

by adding lengths of coaxial cable in between the inputs of the three amplifiers used to acquire the various periods. The cables are of length, *L*, which is roughly equal to a foot. One length of cable was introduced in between the inputs of the modulus-3 and modulus-4 amplifiers. Thus, a delay corresponding to the time to propagate through a length, *L*, of coaxial cable is present. Another cable was introduced in between the modulus-4 and modulus-5 amplifier inputs yielding the same delay between the modulus-4 and modulus-5 folding waveforms. Figure 21 shows the shifted waveforms produced by a time shift between the inputs in Figure 17.

One must be warned that this technique can only be employed with a linearly increasing or decreasing voltage. The input modulating signal used in the ADC was a triangle wave generated by the Agilent 33120A Function/Arbitrary Waveform Generator

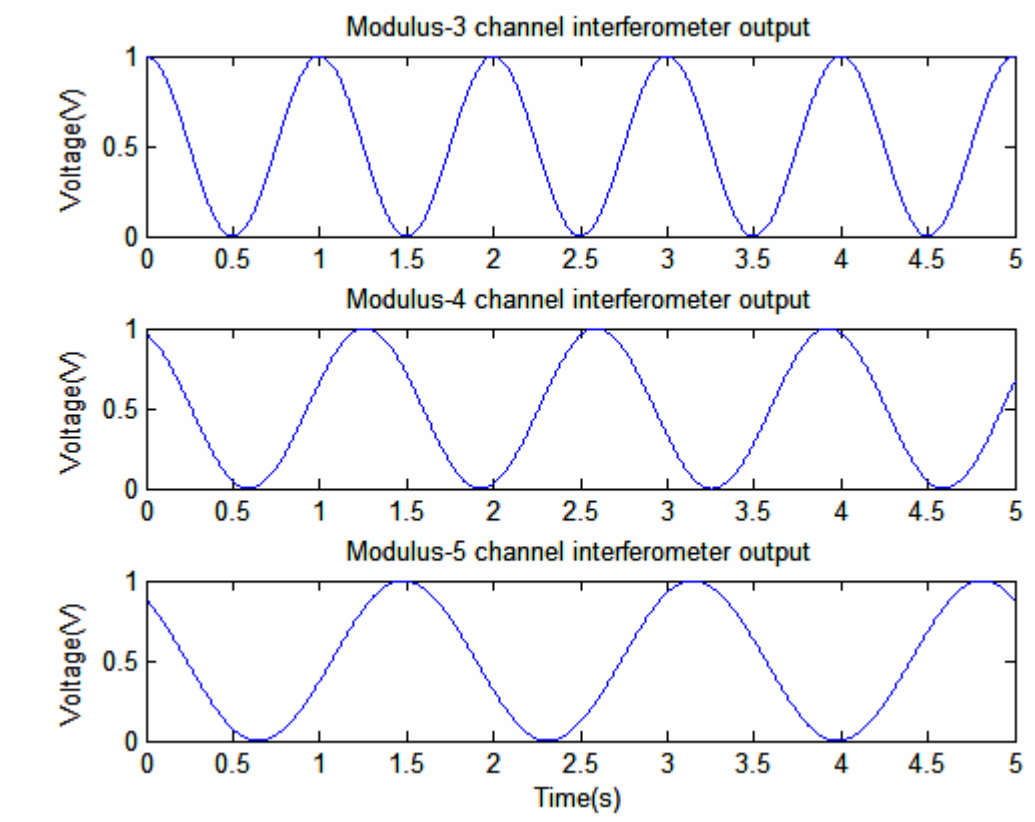

Figure 21. Time-Shifted Modulator Outputs

shown in Figure 22. Since a triangle wave has a linearly increasing voltage, followed by a linearly decreasing voltage, a time delay was an appropriate method for shifting the folding waveforms. The folding waveform generated has the correct phase shift in the linear regions of the triangle waveform. During the times where the triangle waveform transitioned from an increasing signal to a decreasing signal and vice-versa, the shifts were not accurately placed. The amplitude of the triangle wave was more than ample and produced many periods of the folding waveforms.

A time delay is not ideal under normal operation, however. If the modulating signal input to the interferometers were to be a random analog signal, an offset would have to be added after amplification. In this case, a time delay is not a feasible technique.

C. AMPLITUDE ANALYSIS

A 'folded' waveform is acquired through modulating a random RF signal with an MZI. The 'folding' waveforms are acquired using a linearly increasing or decreasing signal as the RF signal. Thus, the 'folding' waveform is a special case of 'folded' waveform that allows the observation of its period and phase. The next aspect of the RSNS physical implementation involves the amplitude sampling of three folded waveforms. After converting each folded waveform to electrical signals, they are fed into three separate banks

Figure 22. Agilent 33120A Arbitrary Waveform Generator

of comparators. Recall that each channel had a number of thresholds equal to its modulus number. These thresholds then determine an element of the digital code word involved in the conversion. Determining where the amplitudes of the folding waveforms are relative to these threshold voltages is the job of the comparator banks. The references of the comparators were set accordingly. For instance, the comparator reference voltages for the modulus-3 channel were set so that the amplitude of the waveforms was divided into four equal ranges. Thus, with an amplitude of +REF Volts, the comparator reference levels were set to $0.25*(+\text{REF})$, $0.50*(+\text{REF})$, and 0.75*(+REF) Volts. Table 4 shows the reference levels for each comparator.

In a given sample, the amplitude of one of the three folding waveforms is determined by the number of comparators that are on in a given channel. For instance, if a sample of the modulus-3 channel yields a 001 for the corresponding states of the comparators, then this correlated to a RSNS row element of 1. Table 5 shows the row element produced for each combination of possible comparator states. In this table, the state of comparator 1 is considered the least significant bit for all three channels.

Modulus-3 Channel	**Reference Voltage**
Comparator 3	0.75*(+*REF*)
Comparator 2	0.50*(+*REF*)
Comparator 1	0.25*(+*REF*)
Modulus-4 Channel	
Comparator 4	0.80*(+*REF*)
Comparator 3	0.60*(+*REF*)
Comparator 2	0.40*(+*REF*)
Comparator 1	0.20*(+*REF*)
Modulus-5 Channel	
Comparator 5	0.83*(+*REF*)
Comparator 4	0.66*(+*REF*)
Comparator 3	0.50*(+*REF*)
Comparator 2	0.33*(+*REF*)
Comparator 1	0.16*(+*REF*)

Table 4. Comparator Reference Voltages

Twelve bits representing the twelve comparator states are sent to a data acquisition device for every sample. A table lookup then converts the comparator states to the correct row element, corresponding to Figure 3. This is the final element of the ADC design, resulting in a digital code word describing the input analog voltage.

Revealed here is a feasible ADC design that maintains the properties of a RSNS scheme utilizing folding waveforms. This chapter illustrates how the properties of the RSNS were obtained with an optical infrastructure. Chapter V discloses the results of the work that was done towards achieving a working physical ADC. The chapter consists of the specifics of the generated folding waveforms as well as the testing of the comparator sampling circuit.

Modulus-3 Channel Row Element	**Comparator States**
0	000
1	001
2	011
3	111
Modulus-4 Channel Row Element	
0	0000
1	0001
2	0011
3	0111
4	1111
Modulus-5 Channel Row Element	
0	00000
1	00001
2	00011
3	00111
4	01111
5	11111

Table 5. Comparator States and Corresponding Row Elements

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V. ADC RESULTS

Chapter IV described the techniques that were used to implement an RSNS ADC using the hardware that was available. Here, the resulting folding waveforms are displayed along with a discussion of how the comparator circuits were programmed and tested.

A. FOLDING WAVEFORMS

As mentioned in Chapter IV, the periods of the folding waveforms were realized through three RF amplifiers. Figure 23 shows the amplifiers that were used. In order to amplify the received analog voltage signal, the signal was sent to the input of three different amplifiers. The gain was adjusted by the knob in the middle of the figure so that the three folding waveform periods could be set correctly. The gain for the modulus-3 channel was set at 6 dB, shown in Figure 23. Gains for the modulus-4 and modulus-5 channels were approximately 4.8 dB and 3.8 dB, respectively.

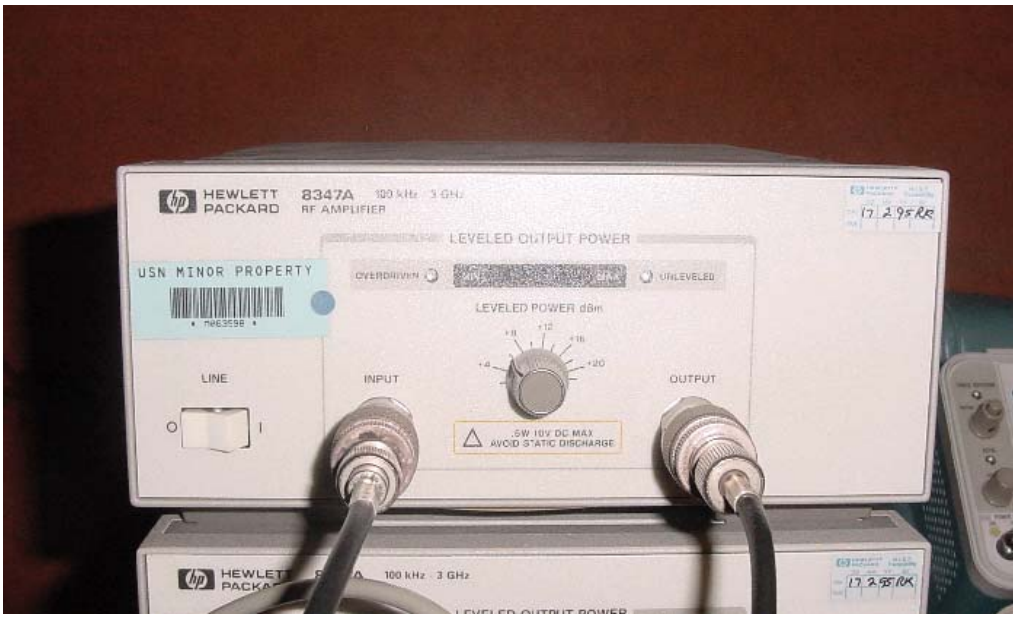

Figure 23. HP 8347A RF Amplifier

Figure 24 includes two oscilloscope displays that show the three folding waveforms. The oscilloscope displayed the waveforms after they were detected and amplified. After amplification, the outputs of the linear amplifiers (shown in Figure) were fed into the oscilloscope. This was done with all three channels.

a)

b)

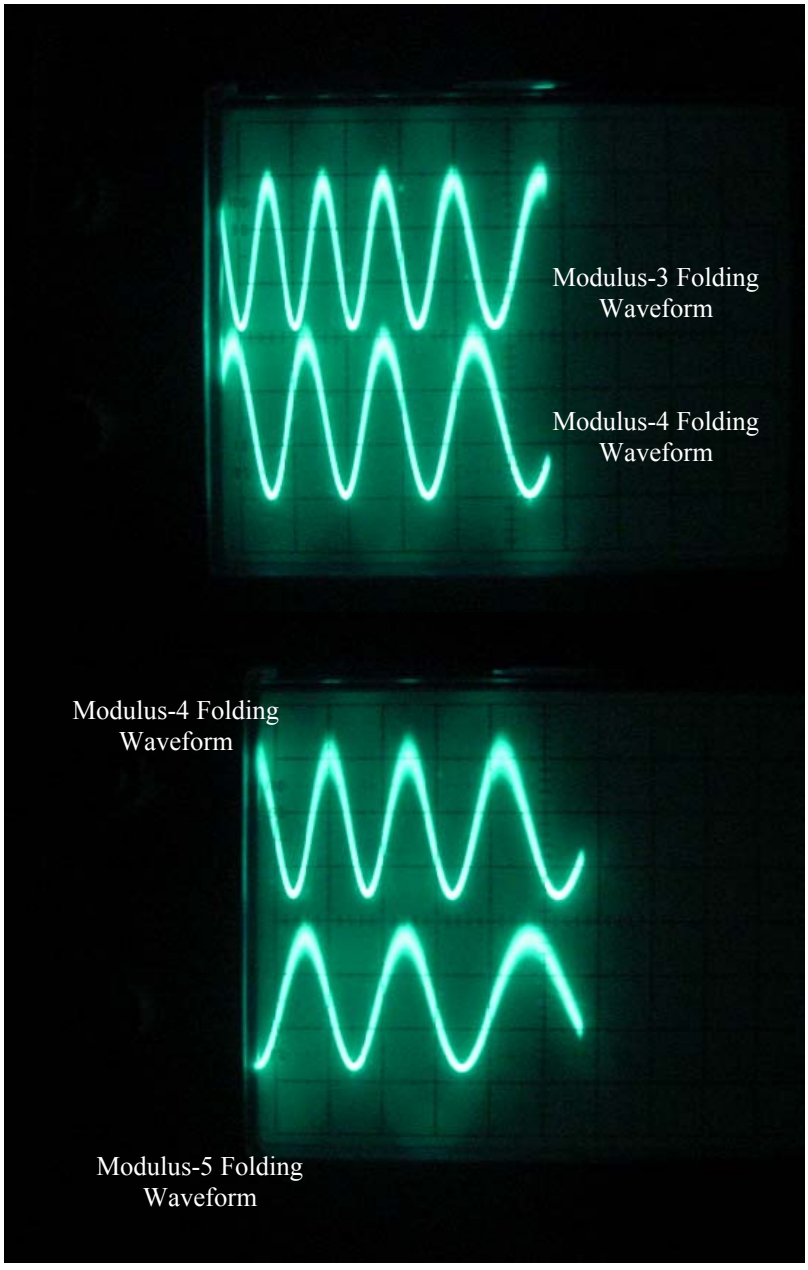

Figure 24. Oscilloscope Displaying a) the Modulus-3 and Modulus-4 Waveforms and b) the Modulus-4 and Modulus-5 Waveforms

The top waveform of the first display is the modulus-3 waveform, and the bottom the modulus-4 waveform. The modulus-4 waveform was shown again at the top of the second display. This was done so that the periods could be compared. The modulus-4 waveform is shown with a different phase in the two displays. This is because the triggering of the oscilloscope was different in each display. The horizontal scale of the display was set to 0.5 ms per division. That said, the periods of the waveforms shown are 0.6 ms, 0.8 ms, and 1.0 ms, respectively. Shifting the waveforms was accomplished using variable lengths of coaxial cable before the RF signal amplification to introduce time delays. This was far from exact, and can be assumed a rough estimate. However, the waveforms in Figure 24 show that the peaks and nulls never occur at the same instance, which prove that shifts are present.

B. COMPARATOR CIRCUIT TESTING

The comparator circuit board, shown again in Figure 25, amplitude-analyzes

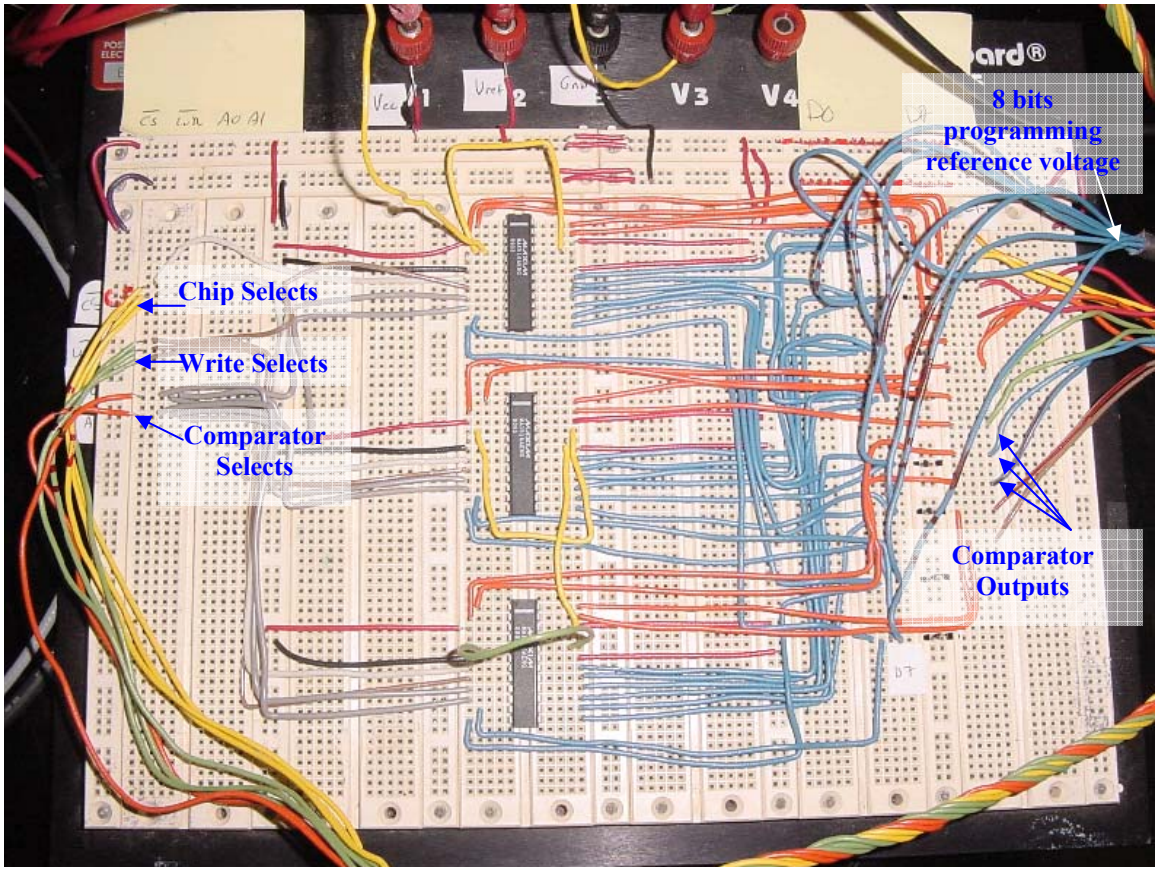

Figure 25. Comparator Bank Circuit

the folded waveforms produced in the previous section. To test the functionality of the comparator circuit, a DAQPad-6507, shown in Figure 26, was used to interface the circuit with the computer program, LabView. LabView not only aided in testing the operation of the comparator chips, but also facilitated the setting of the comparator threshold values.

A total of 28 lines were used for the transfer of digital data to and from the comparator board. Sixteen of them were used for the setting of threshold voltages, while the remaining 12 were used to continuously read the comparator states.

The first 16 lines were split into two ports of 8. The first port was used to systematically set the chip, write, and comparator selects. Values for the comparator threshold voltages were then fed through the remaining 8 lines. A different comparator threshold voltage was sent for each comparator, so the code words sent through the first port and the second port had to be timed precisely.

Figure 26. National Instruments DAQPad-6507

Using the DAQPad in Figure 26, a program was created in LabView to send a series of digital words so that the threshold values would be set. A screen capture of the program is shown in Figure 27. In this program, a total of 50 8-bit binary words were sent to each port. At the left of the screen capture, there are two arrays where the 8-bit binary values can be set. The top array is configured to send the chip, write, and comparator select information. Threshold voltage levels are sent through the bottom array. In each array, there are two numbers. The first labels which element of the array is being displayed (ranges from 0-49). The second number is the 8-bit array element shown in base 10 (255 corresponds to 8 digital ones). These arrays are then concatenated by the program and sent out to the comparator board two elements at a time, one for each port.

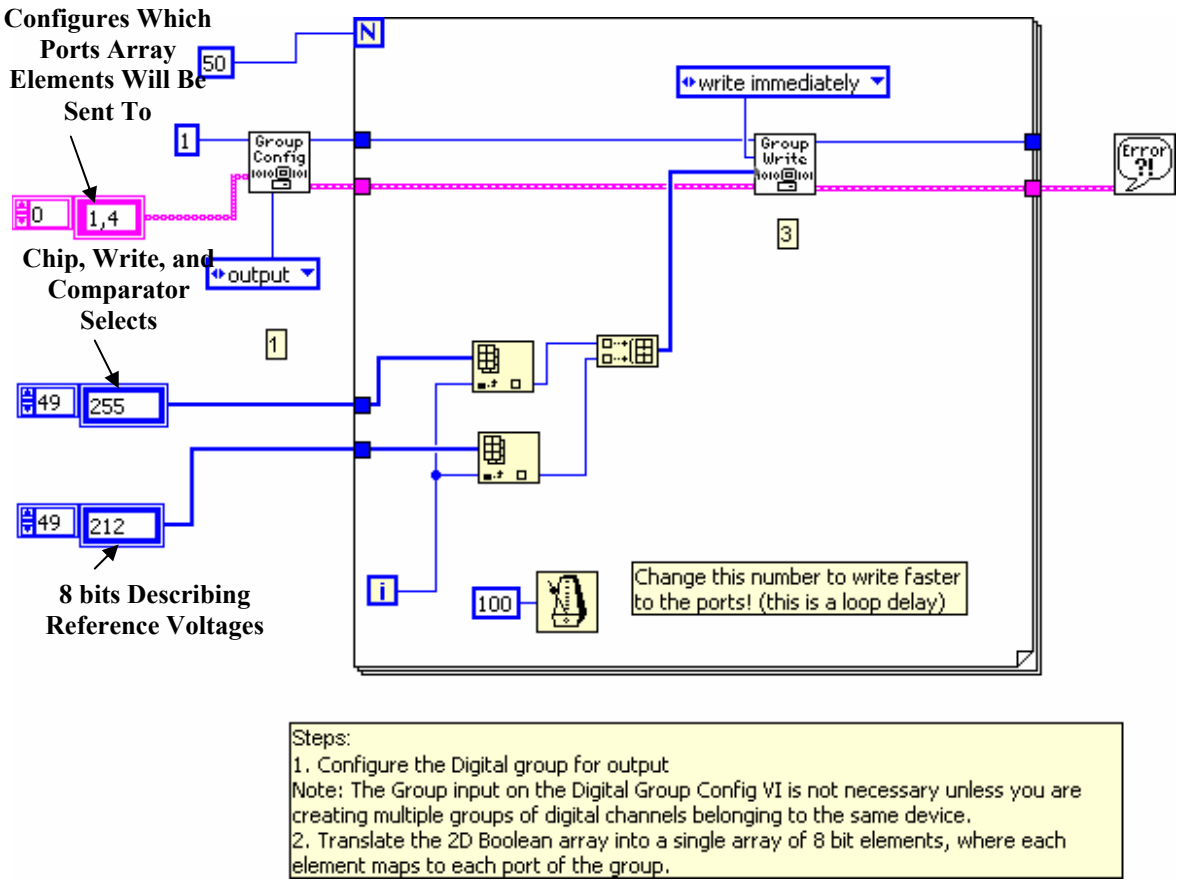

Figure 27. Screen Capture of LabView Program That Sets Threshold Voltages

A second program was used to continuously read the states of the comparator. The screen capture of this program is shown in Figure 28. In this program, a sample is

taken every 1 ms. The sample rate is set by the loop delay shown in the screen capture. For each sample, the comparator states are read are displayed using rows of LEDs. The LEDs are not physical LEDs but rather show up on the computer screen as LEDs that light up green when a comparator ON state is received, and light up red when a

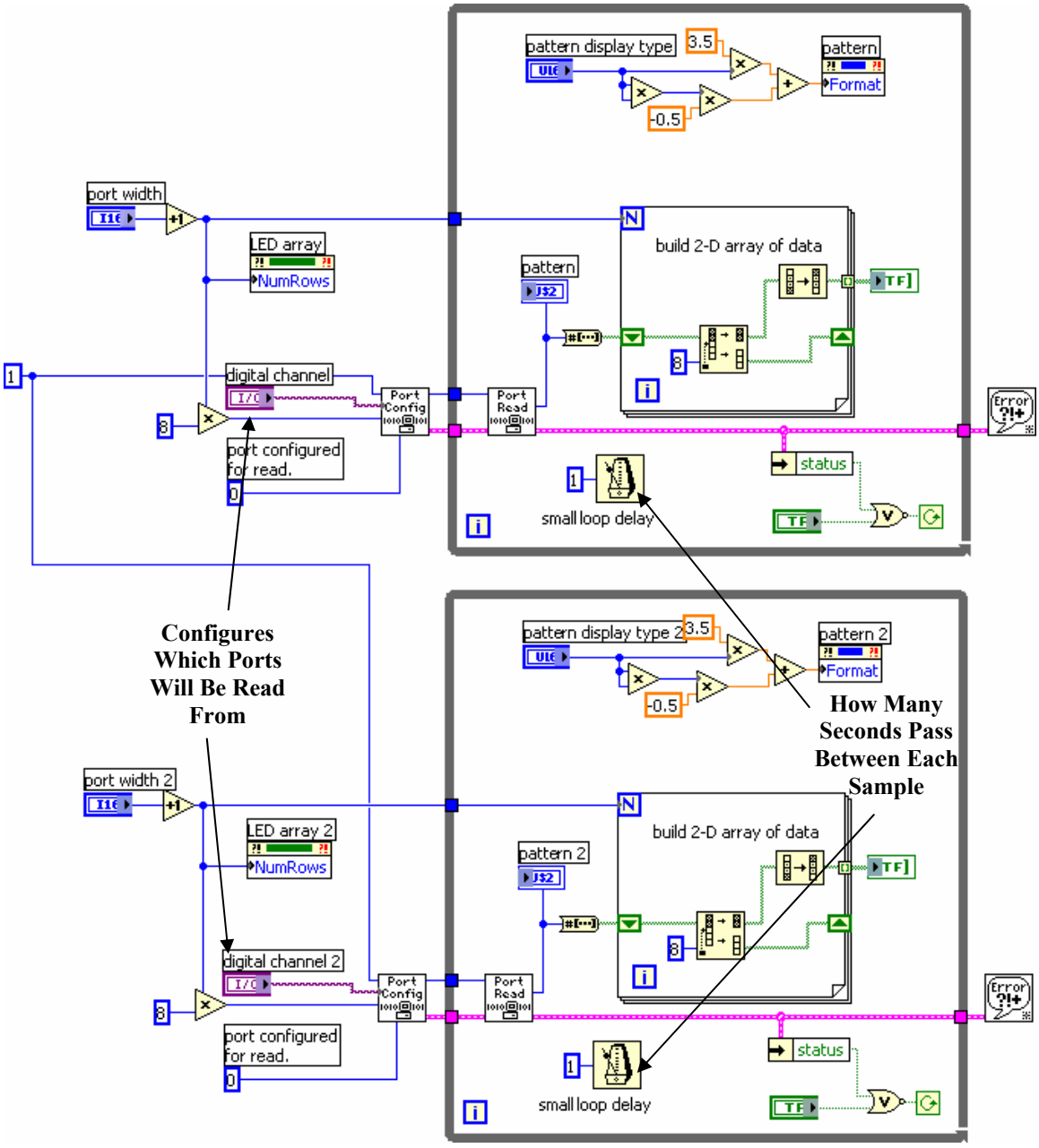

Figure 28. Screen Capture of LabView Program That Reads Comparator States

comparator OFF state is received. To test the operation of the comparator circuits, a voltage input to the comparators was needed. The most useful device available was a Global Specialties Model 1300 Power Supply, shown in Figure 29. Acting as a DC voltage source, this device allows the user to control the input voltage to the comparators. Thus, with the program that reads comparator states running, the user can witness the changing of the comparator states as the input DC voltage changes. Figures 30 and 31 show the arrays of LEDs at different times while the program was running.

Figure 29. Global Specialties Model 1300 Power Supply

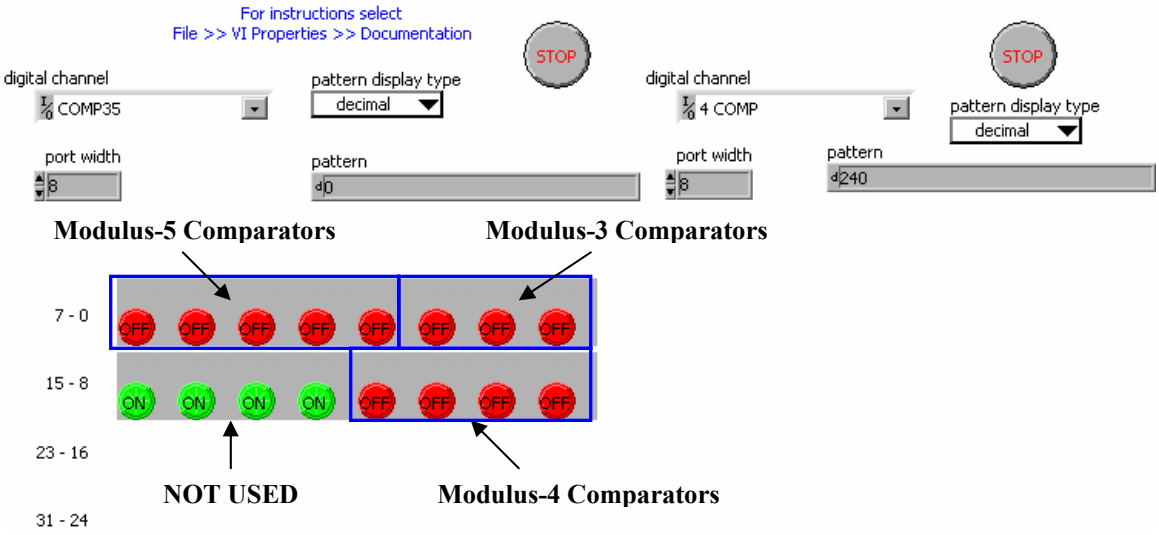

Figure 30. LabView Screen Capture Showing the Comparator States with an Input DC Voltage of 0 V.

In this case, the input voltage provided by the power source was input into all 12 comparators simultaneously. With the entire ADC running properly, the voltage inputs to the comparator banks would differ based on the three folding waveforms. The inputs were made the same for testing purposes. As the DC voltage increased, all 12 comparator states changed accordingly. Figure 31 displays how the comparators changed states at an input voltage of 2.6 V. The range of input voltage values that the comparators were to detect is REF=5 V. Thus, with an input voltage of 2.6 V, every comparator that has a threshold voltage of less than $\left(\frac{2.6V}{5.0V}\right)$*REF should be in the ON state. Figure 31 verifies that the comparators respond in this way. For instance, in the Modulus-5 comparator bank, the comparators with the lowest three threshold voltages are in the ON state. Since the middle LED (of the five in the Modulus-5 comparator bank) represents the comparator with a threshold voltage of 0.5*REF, which is less than $\left(\frac{2.6V}{5.0V}\right)$*REF, the LED should be ON. The same is true for the other two LEDs, representing comparators of threshold voltages of 0.33*REF and 0.16*REF, respectively.

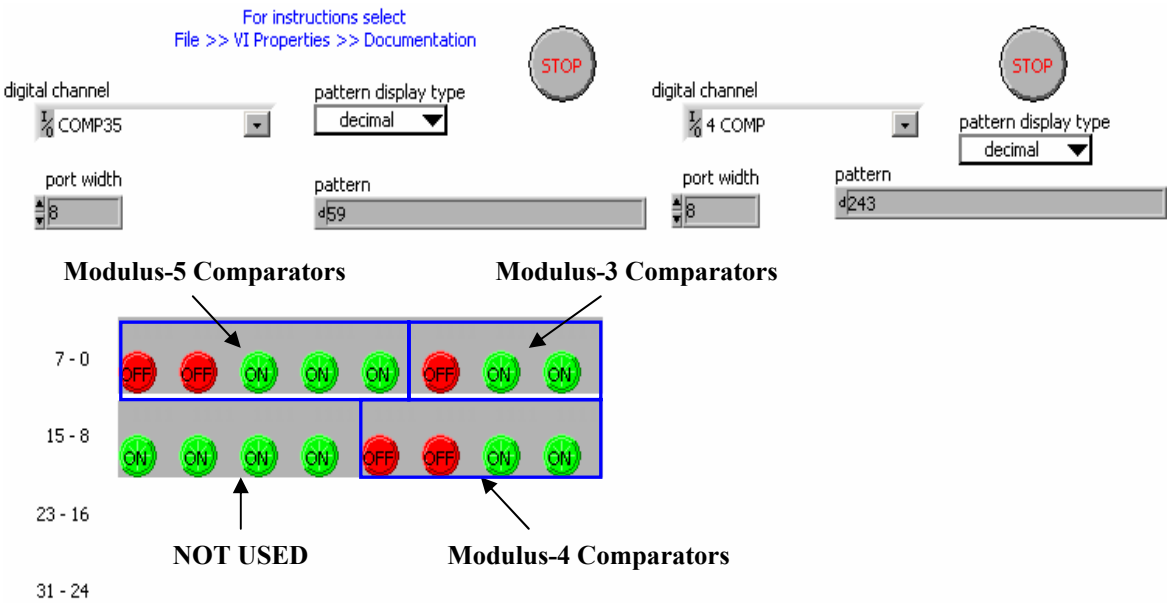

Figure 31. LabView Screen Capture Showing the Comparator States with an Input DC Voltage of 2.6 V.

With the folding waveforms generated and the comparator circuit functioning properly, the only step left is to feed the folding waveforms into the input pins of the comparator banks. However, a drawback was encountered when trying to do this. The LabView program that reads the comparator states can only read the states once every 1 ms (equivalent to a sampling rate of 1 kHz). This is a problem considering the triangle wave that served as the analog received voltage source was 100 kHz. This value had to be used because the amplifiers that adjusted the periods of the folding waveforms had a bandwidth ranging from 100 kHz to 1 GHz. In order to sample the resulting folding waveforms effectively, a sampling rate of around 2-3 MHz is required. Not only was the software lacking in its ability to make the DAQPad-6507 sample that fast, but the USB cable that runs between the computer and the DAQPad-6507 significantly lacks the bandwidth required to carry samples at rates that high. Though the operation of the RSNS ADC was verified, a device with a higher sampling rate is required for a full implementation.

This chapter described what was accomplished in this thesis. Chapter VI concludes this thesis by featuring the accomplishments and implications of this design.

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VI. CONCLUSION

As the rate of analog-to-digital conversion is increased due to improved technologies and techniques, ADCs will need to perform better in areas such as resolution and robustness as well. This thesis demonstrated how a RSNS ADC architecture can offer these qualities. The resolution of the architecture is accomplished due to the minimal number of comparators that are needed to achieve a high resolution. An RSNS-encoded scheme also provides robustness. This means that the system can handle errors and still perform well due to its inherent Gray-code properties.

An RSNS ADC architecture was constructed and tested. Operation of the ADC prototype was verified by observing the produced folding waveforms and proving the functionality of the comparator circuits.

There are many aspects of this work that can be improved upon. For a fully completed RSNS ADC, the shifting in phase of the waveforms relative to another must be done with an introduced DC offset. This is contrary to the time delay technique that was used here. An offset must be used because the input analog voltage to the ADC will not necessarily be a steadily changing voltage. The signal received will most likely have many random qualities, making the time delay ineffective.

Another aspect that should be improved is the accuracy of the folding waveforms. The periods of the folding waveforms were set using the gain dials on three amplifiers. An amplifier with a higher degree of precision would be useful in providing more exact periods. Having an accurate set of folding waveforms is necessary if the ADC is to perform at a high rate of conversion.

The comparator circuit that was used to read in the folding waveforms operates well. Comparator threshold voltages were set according to folding waveforms with a triangle wave shape. In this implementation, the MZIs produce waveforms with a cosine squared wave shape. Thus, the threshold levels need to be modified so that each least significant bit will correspond to a consistent range of input voltage.

Carrying out the full operation of the prototype would include an improved sampling device. This device will need to interface with the computer as well. LabView has the capability of sampling at higher rates given the access to some improved data acquisition equipment.

The completion of this prototype is important on many levels. Better resolution and robustness are two of the advantages of the RSNS encoding. Coupled with the high bandwidth and low loss characteristics of optical fiber and components, this ADC has the potential to be an important step towards realizing ADCs of unrivaled capabilities.

APPENDIX

The Appendix consists of the data sheets for the MAX516 Quad-Comparator with Programmable Threshold device.

19-4446; Rev 1; 8/94

MAXIM

Quad Comparator with Programmable Threshold

MAX516

General Description

The MAX516 combines four low-power, programmable-threshold comparators on a single CMOS IC. Separate 8-bit digital-to-analog converters (DACs) drive the comparator inverting (-) inputs so that individual trip thresholds can be digitally set. All noninverting (+) comparator inputs are brought out as analog inputs (AIN0-AIN3). Each comparator output swings high when its analog input exceeds its digitally set threshold. All four DACs share a common reference input to optimize matching and eliminate external trims.

Digital inputs and comparator outputs are compatible with TTL and CMOS logic. A separate logic supply (V_{CC}) allows comparator output levels to be set independently of V_{DD}. The MAX516 operates conveniently from a single supply with V_{DD} tied to V_{CC}. Commercial, extended, and military temperature ranges are provided in 24-pin narrow DIP and wide SO packages.

Applications

Window Comparators

Power-Supply Monitors

Alarm Limit Detectors

Battery Chargers

Automated Test Equipment

Process Control

Features

- ♦ 4 Comparators and 4 DACs
- ♦ Digitally Set Threshold
- ♦ Monotonic Over Temperature
- ♦ Parallel Microprocessor Interface
- ♦ +5V to +15V Supply Operation

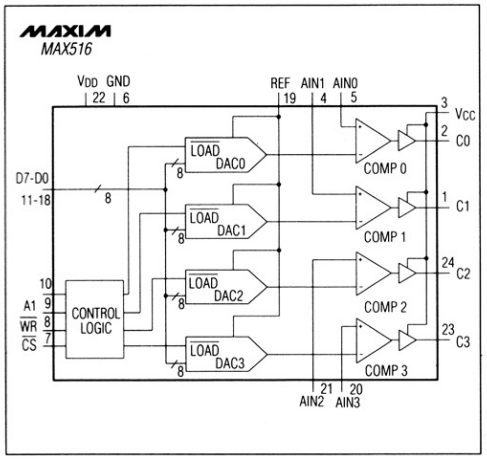
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX516ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX516BCNG	0°C to +70°C	24 Narrow Plastic DIP	±2
MAX516ACWG	0°C to +70°C	24 Wide SO	±1
MAX516BCWG	0°C to +70°C	24 Wide SO	±2
MAX516BC/D	0°C to +70°C	Dice*	±2
MAX516AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX516BENG	-40°C to +85°C	24 Narrow Plastic DIP	±2
MAX516AEWG	-40°C to +85°C	24 Wide SO	±1
MAX516BEWG	-40°C to +85°C	24 Wide SO	±2
MAX516AMRG	-55°C to +125°C	24 Narrow CERDIP**	±1
MAX516BMRG	-55°C to +125°C	24 Narrow CERDIP**	±2

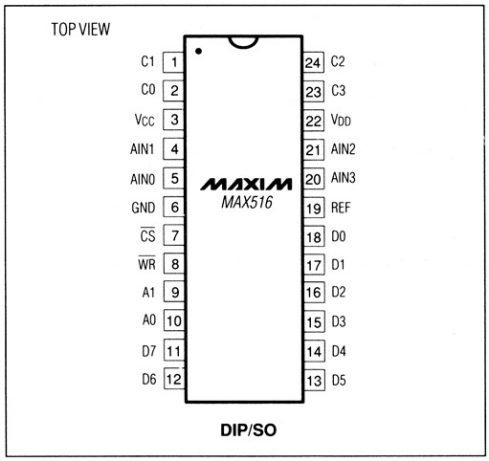
** Contact factory for dice specifications.*

*** Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configuration



Quad Comparator with Programmable Threshold

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V, +17V
V_{CC} to GND .....-0.3V, V_{DD} + 0.3V
V_{DD} to V_{CC} .....-0.3V, +17V
Digital Input Voltage to GND .....-0.3V, V_{DD} + 0.3V
REF to GND .....-0.3V, V_{DD} + 0.3V
Comparator Input to GND.....-0.3V, V_{DD} + 0.3V
C0–C3 to GND (Note 1) .....GND, V_{CC} + 0.3V
Continuous Current V_{CC} or GND 12mA

Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 8.7mW/°C above +70°C)..480mW
Wide SO (derate 11.8mW/°C above +70°C).....650mW
Narrow CERDIP (derate 12.5mW/°C above +70°C) 690mW
Operating Temperature Ranges:
MAX516_C_ .....0°C to +70°C
MAX516_E_.....-40°C to +85°C
MAX516_MRG .....-55°C to +125°C
Store Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: The outputs may be shorted to GND or V_{DD}, provided the package's power dissipation is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = +4.75V, REF = +1.25V or V_{DD} = V_{CC} = +16.5V, REF = +10V; GND = 0V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			8			Bits
Total Unadjusted Error	TUE	MAX516A				±1	LSB
		MAX516B				±2	
Relative Accuracy	INL	MAX516A				±0.5	LSB
		MAX516B				±1	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Full-Scale Error		MAX516A				±0.5	LSB
		MAX516B				±1	
Full-Scale Temperature Coefficient		V_{DD} = 15V, REF = 10V			±5		ppm/°C
Zero-Code Error		T_A = +25°C	MAX516A			±5	mV
		T_A = T_{MIN} to T_{MAX}	MAX516A			±10	
		T_A = +25°C	MAX516B			±10	
		T_A = T_{MIN} to T_{MAX}	MAX516B			±15	
Zero-Code Temperature Coefficient					±30		µV/°C
REFERENCE INPUT (4.75V ≤ V_{DD} ≤ 16.5V)							
Reference Input Range	REF			1.25		V_{DD} -3.50	V
Reference Input Resistance	RREF	Worst-case code		3.0	4.5		kΩ
Reference Input Capacitance	CREF	Worst-case code (Note 2)			100	250	pF
COMPARATOR INPUT (4.75V ≤ V_{DD} ≤ 16.5V)							
Comparator Input Range	V_{AIN}			0		V_{DD}	V
Comparator Input Bias Current	I_B	T_A = +25°C			50	300	nA
		T_A = T_{MIN} to T_{MAX}			100	400	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = V_{CC} = +4.75V, REF = +1.25V or V_{DD} = V_{CC} = +16.5V, REF = +10V; GND = 0V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

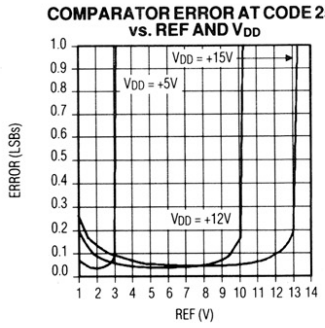
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS D0–D7, $\overline{WR}$, $\overline{CS}$, (4.75 ≤ V_{DD} ≤ 16.5V)						
Input High Voltage	V_{INH}		2.4			V
Input Low Voltage	V_{INL}				0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}			±1	µA
Input Capacitance	C_{IN}	(Note 2) All except MAX516_MRG			10	pF
		(Note 2) MAX516_MRG			15	pF
DIGITAL OUTPUTS C0–C3 (V_{CC} = 5V)						
Output High Voltage	V_{OH}	I_{SOURCE} = 200µA	V_{CC} - 1			V
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA			0.4	V
DYNAMIC PERFORMANCE (1.25V ≤ REF ≤ V_{DD} - 3.5V, 0V ≤ AIN < V_{DD} -2V)						
Digital Input to Comparator Out Delay	t_{DCO}	(Note 3)		0.8	2.0	µs
Analog Input to Comparator Out Delay	t_{ACO}	(Note 4)		0.8	1.5	µs
TIMING CHARACTERISTICS						
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_{CS}		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_{CH}		0			ns
Address to $\overline{WR}$ Setup Time	t_{AS}		50	30		ns
Address to $\overline{WR}$ Hold Time	t_{AH}		5	0		ns
Data Valid to $\overline{WR}$ Setup Time	t_{DS}		50	30		ns
Data Valid after $\overline{WR}$ Hold Time	t_{DH}		5	0		ns
$\overline{WRITE}$ Pulse Width	t_{WR}		120	50		ns
POWER SUPPLIES						
V_{DD} Range	V_{DD}		4.75		16.5	V
V_{CC} Range	V_{CC}		4.75		V_{DD} + 0.30	V
Positive Supply Current	I_{DD}	Logic inputs < V_{IL} or > V_{IH}			10	mA
Logic Supply	I_{CC}				10	µA

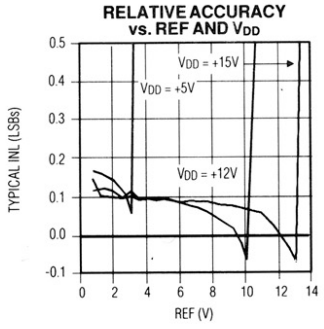
Note 2: Guaranteed by design. Not production tested.

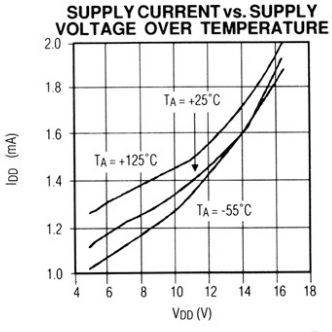
Note 3: V_{DD} = 5.00V, differential comparator input voltage changes by 1.25V with 5mV overdrive. V_{IN} must be 3.5V less than V_{DD}, or longer propagation delays will result.

Note 4: Not tested, but guaranteed by correlation to t_{DCO}.

Typical Operating Characteristics







Quad Comparator with Programmable Threshold

Pin Description

PIN	NAME	FUNCTION
1, 2	C1, C0	Comparator Outputs
3	V_{CC}	Comparator Output Supply
4, 5	AIN1, AIN0	Comparator Analog Inputs
6	GND	Ground
7	$\overline{CS}$	CHIP SELECT
8	$\overline{WR}$	WRITE
9, 10	A1 , A0	DAC Address Inputs
11-18	D7-D0	DAC Data Inputs, 8 bits
19	REF	Reference Input
20, 21	AIN3, AIN2	Comparator Analog Inputs
22	V_{DD}	Positive Supply Voltage
23, 24	C3, C2	Comparator Outputs

Detailed Description

The MAX516 contains four analog comparators and four matched 8-bit digital-to-analog converters (DACs). The voltage output of each DAC is expressed in the equation:

$$V_{DAC} = REF \times N/256,$$

where N is the numerical equivalent of the 8-bit DAC input code (D0-D7). N ranges from 0 to 255 and may be set to a different level for each DAC (Table 1). The DAC output, V_{DAC}, does not appear on an output pin of the MAX516 but is instead compared to an analog input signal by one of four internal comparators (see *Functional Diagram*). A comparator output is high when AIN is more positive than the comparator's digitally set threshold.

Table 1. Comparator Threshold vs. DAC Input Code

DAC CODE MSB	DAC CODE LSB	COMPARATOR THRESHOLD
1111	1111	$+REF\left(\frac{255}{256}\right)$
1000	0001	$+REF\left(\frac{129}{256}\right)$
1000	0000	$+REF\left(\frac{128}{256}\right) = +\frac{REF}{2}$
0111	1111	$+REF\left(\frac{127}{256}\right)$
0000	0001	$+REF\left(\frac{1}{256}\right)$
0000	0000	0V

NOTE: $1LSB = (REF)(2^{-8}) = +REF\left(\frac{1}{256}\right)$

Reference Input

Comparator trip thresholds vary digitally between 0V and 1LSB below REF. All DACs share the same reference input.

The input impedance of REF is code dependent. The lowest impedance, typically 2kΩ, occurs when 0101 0101 (HEX 55) is loaded into D0-D7 on all four DACs. When 0000 0000 is loaded into all DACs, REF appears as an open circuit. Because the input resistance at REF is code dependent, the reference source should have an output impedance of no more than 4Ω to maintain linearity. Input capacitance at REF is also code dependent and typically varies between 100pF and 250pF.

Comparator Inputs

The "+" input of each comparator is brought out to AIN0-AIN3. Comparator input bias current is typically 100nA. Analog source resistances below 1.25kΩ generate less than 250μV of bias-current induced comparator offset error.

Digital Interface

The digital inputs (D0-D7, $\overline{CS}$, $\overline{WR}$) are both TTL and 5V CMOS logic compatible; however, the power-supply current, I_{DD}, depends on input logic levels. Supply currents will be highest with TTL levels (tested limits are with worst-case logic levels). Supply current is reduced when digital inputs are driven near GND and above 4V.

Address lines A0 and A1 select which DAC receives data from the input port. Because $\overline{CS}$ and $\overline{WR}$ are internally ORed, the write cycle begins only after both go low, but data is latched and transferred to a DAC when either input returns high. Figure 1 shows the input control logic, Table 2 lists DAC addresses, and Table 3 is the truth table for $\overline{WR}$ and $\overline{CS}$. Figure 2 shows write-cyle timing.

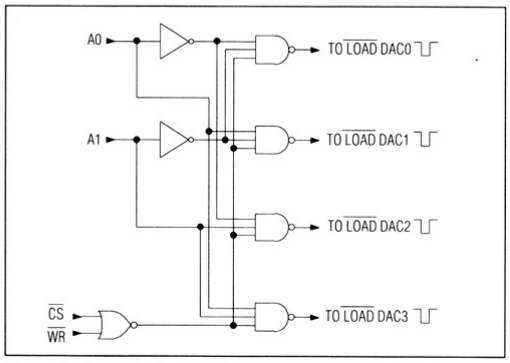


Figure 1. Input Control Logic

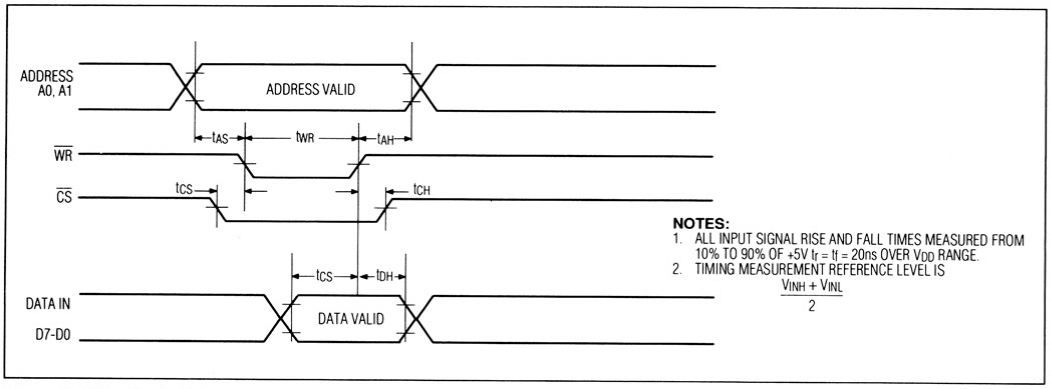


Figure 2. Write-Cycle Timing

Table 2. DAC Addressing

A1	A0	SELECTED DAC
0	0	DAC0 Input Register
0	1	DAC1 Input Register
1	0	DAC2 Input Register
1	1	DAC3 Input Register

Table 3. Write-Cycle Truth Table

$\overline{CS}$	$\overline{WR}$	FUNCTION
1	X	No operation. The MAX516 is deselected. Existing register contents remain unchanged.
0	0	DAC contents for selected address are loaded, but do not update the DAC until WR goes high.
0	↑	Latch D0-D7 into input register of the selected DAC on rising edge.

NOTES: X = Don't Care, ↑= Rising Edge

Applications Information

Power-Supply and Reference Operating Ranges

The MAX516 is fully specified to operate with V_{DD} between +4.75V and +16.5V and is specified to operate with a reference input range of +1.25V to V_{DD} -3.5V.

The comparator output supply, V_{CC}, has a range of +4.5V to (V_{DD} + 0.3V). This allows the comparators' logic-high output levels to be set independently from V_{DD}. In most applications, simply connect V_{CC} and V_{DD} together. Comparator outputs typically swing within 200mV of the supply rails when loaded with CMOS logic inputs.

Hysteresis

When analog input signals are slow moving or contain noise, comparator outputs may "chatter" near the threshold point. Be sure that proper power-supply bypass capacitors are in place (see *Grounds and Bypassing* section), because supply current rises when an output switches.

Hysteresis may be added to any or all comparators to further resist oscillation during output transitions. This is accomplished with two resistors, as shown in Figure 3. When hysteresis is added, the threshold point will shift slightly as a result of the voltage divider formed by R1 and R2. The amount of shift is described below:

$$V_{TH} = V_T\left(\frac{R1}{R2} + 1\right)$$

$$V_{TL} = V_T\left(\frac{R1}{R2} + 1\right) - V_{CC}\left(\frac{R1}{R2}\right)$$

$$V_{HYST} = V_{TH} - V_{TL}$$

$$V_{HYST} = V_{CC}\left(\frac{R1}{R2}\right)$$

V_T is the threshold voltage set by the internal DAC with no hysteresis connected. V_{TH} is the shifted high-going threshold with hysteresis added. V_{TL} is the shifted low-going threshold with hysteresis. V_{HYST} is the total hysteresis and equals V_{TH} - V_{TL}. Note that V_{TL} and V_{HYST} change with V_{CC}. With V_{CC} = 5V, R1 = 1kΩ, and R2 = 200kΩ, V_{HYST} = 25mV. Even though R1 is relatively small, the impedance seen by the signal source is large: R1 + R2. However, if R1 is large, input bias current (400nA

Quad Comparator with Programmable Threshold

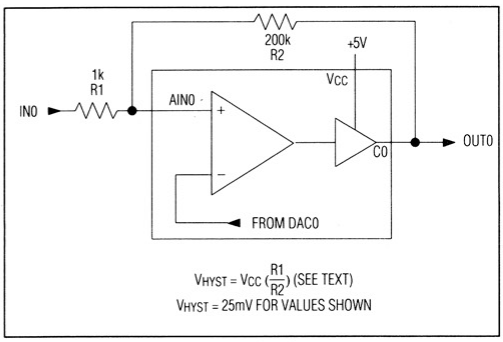


Figure 3. Adding Hysteresis to Any Comparator

max over temp.) may add offset error. 1kΩ x 400nA = 0.4mV offset error is due to bias current.

Grounds and Bypassing

Careful PC-board layout significantly minimizes crosstalk among the reference input, comparator outputs, and digital inputs. Keep digital and analog lines separate, and use ground traces as shields between them where possible. Separate AIN0-AIN3 and REF from each other by running a ground trace between these pins.

Bypass both V_{DD} and V_{CC} to GND with a combination of a 0.1µF low ESR and a 4.7µF capacitor close to the device. If V_{DD} and V_{CC} are connected together, only one set of bypass capacitors is needed. If REF is not an AC input, it should be bypassed as well. Keep bypass-capacitor leads short for best supply noise rejection.

Applications

Threshold detection is often useful in automated test applications. Four individual thresholds can be independently altered under software control.

Figure 4 shows the connection for a hardware window comparison. DAC0 provides the upper trip point, DAC1 the lower trip point. The difference between the trip points is the window size. The AIN0 and AIN1 inputs are tied together. One logic output is inverted and then ORed with the noninverted comparator output. The window output goes high when the analog input sits between the thresholds set by DAC0 and DAC1. The external logic in Figure 4 can also be simulated in software, or use a single comparator to perform a window comparison by loading two threshold limits in succession and noting the comparator results of each (Figure 5).

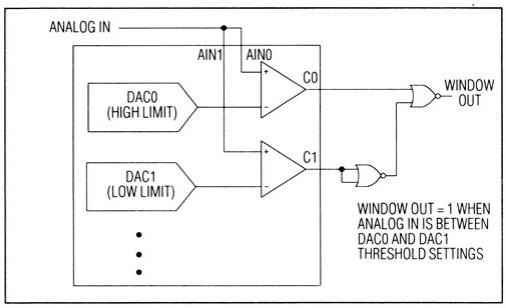


Figure 4. Window Comparison

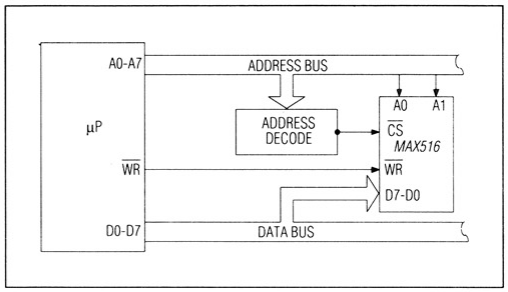
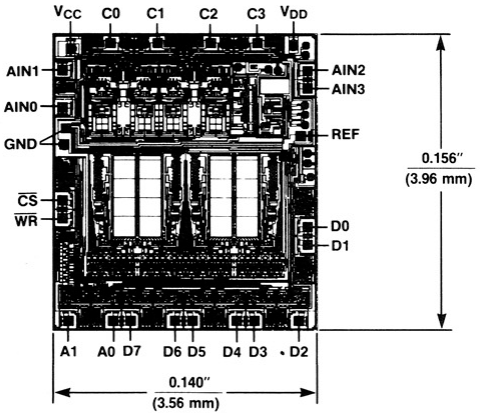
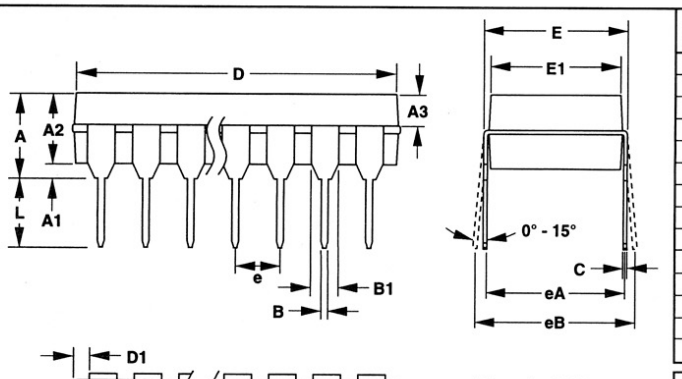


Figure 5. Microprocessor Interface

Chip Topography



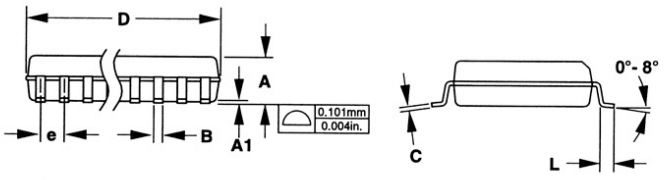
NOTE: Substrate connected to V_{DD}

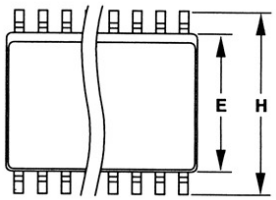


Plastic DIP PLASTIC DUAL-IN-LINE PACKAGE (0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.348	0.390	8.84	9.91
D	14	0.735	0.765	18.67	19.43
D	16	0.745	0.765	18.92	19.43
D	18	0.885	0.915	22.48	23.24
D	20	1.015	1.045	25.78	26.54
D	24	1.14	1.265	28.96	32.13





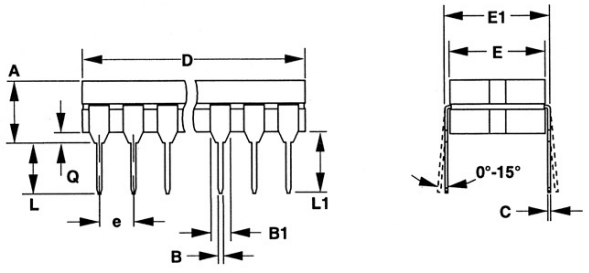
Wide SO SMALL OUTLINE PACKAGE (0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

21-0042A

Quad Comparator with Programmable Threshold



CERDIP
CERAMIC DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.098	–	2.49
S1	0.005	–	0.13	–

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	–	0.405	–	10.29
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51

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